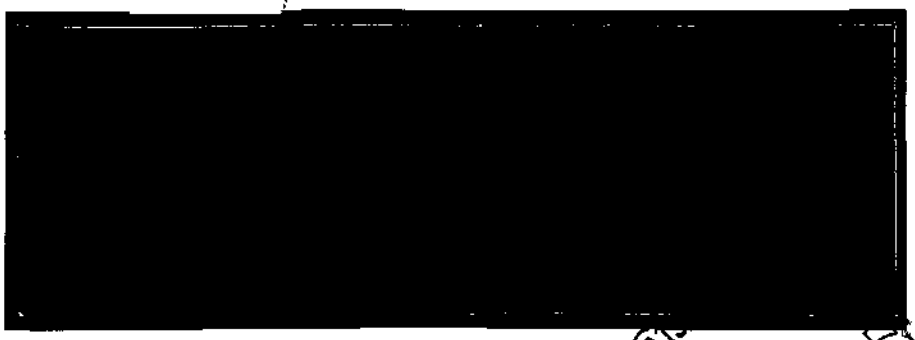

ELECTRICAL ENGINEERING

ENGINEERING EXPERIMENT STATION

AUBURN UNIVERSITY

AUBURN, ALABAMA

A STUDY OF POWER CONDITIONING AND POWER DISTRIBUTION AND COMPONENTS

FINAL REPORT

PREPARED BY
ELECTRONIC SYSTEMS LABORATORY
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JANUARY 1973

CONTRACT NAS8-26752
GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

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FOREWORD

This report is a technical summary presenting the results of a study by the Electronic Systems Laboratory of the Electrical Engineering Department, Auburn University under the auspices of the Engineering Experiment Station. The report is submitted in partial fulfillment of the requirements of Contract NAS8-26752.

ACKNOWLEDGMENT

A dissertation submitted by Hubert Merrill Horton to the Graduate Faculty of Auburn University in partial fulfillment of the requirements for the degree of Doctor of Philosophy is based on the work reported herein. Professor M. A. Honnell served as Mr. Horton's major professor.

A STUDY OF POWER CONDITIONING AND POWER DISTRIBUTION AND COMPONENTS

M. A. Honnell and H. M. Horton

ABSTRACT

The results of a comprehensive simulation and analysis performed on the operation of the regulator part of the Charger/Battery/Regulator Module (CBRM) are detailed in this study. The CBRM is utilized as an integral component of the Skylab/Apollo Telescope Mount (ATM) electrical power system and contains a switching mode electronic regulator. Implementing circuit analysis techniques, pertinent voltages and currents are calculated; these, in turn, are incorporated into the regulator system study. Investigation of the turn-on and turn-off times associated with the switching circuitry is performed and an examination is made on these calculations.

A computer program has been developed to provide a simulation of the switching regulator; this modeling is accomplished using the Fortran language and is processed on the IBM 360/50 computer. The inherent flexibility of the program allows changes in not only the input voltage and load resistance, but the important circuit component values as well.

The simulation model computer program is utilized to generate graphs that will relate various CBRM parameters to one another. Through such graphs, the program will investigate the effects on output voltage,

output power, switching frequencies, and timing pulse-widths as input voltage and load resistance conditions are varied.

The Skylab/ATM has a complex electrical power system network; eighteen CBRM's are electrically connected in parallel and administered by a power sharing circuit. In order to analyze this parallel power-sharing arrangement, control techniques were employed and a feedback diagram was developed. Utilizing this feedback diagram, the system output voltage and individual regulator currents could now be formulated in termes of load resistances, distribution line resistances, and two intrinsic properties of the individual regulators: the output resistance and the no-load output voltage.

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LIST OF FIGURES

I. INTRODUCTION

This report represents the results of a study made on the switching regulator of the Charger/Battery/Regulator Module (CBRM) which is a part of the Skylab/Apollo Telescope Mount (ATM) electrical power system. Eighteen such regulators, which supply common output buses, exist in the ATM and receive their energy from banks of solar cells. Basically, the regulator operates on the principle that a constant output voltage can be obtained at the output of a low-pass filter, if energy is correctly supplied to its input in pulses rather than continuously. The majority of switching regulators come under one of two classes of timing control: 1) those having a constant on pulse-width and a variable switching repetition rate; and 2) those having a constant switching repetition rate and a variable on pulse-width. In the CBRM regulator both the on pulse-width and the switching repetition rate are variable.

To provide the reader with an understanding of the CBRM's overall operation, a simplified functional block diagram is presented and discussed in Chapter II. Also discussed are four basic possible configurations of the output stage of a switching regulator. Chapter III contains the development of mathematical expressions for the currents and voltages associated with the regulator and expressions for the switching times which produce these currents and voltages.

Using the information obtained in Chapter III, a computer program model of the CBRM regulator was developed and is presented in Chapter IV. Also included in that chapter is a discussion of the structure or format of the program and the first two pages of a typical output. The following are four features considered desirable in the computer program and consequently served as a guide during its construction.

1) Furnish all voltages and currents pertaining to the output filter.
2) Furnish output switching transistors' on time and dwell time, and furnish discharge time of the charging inductor.
3) Provide a means of analyzing the load sharing properties of the regulator.
4) Be versatile in format to allow changes in component values and input parameters.

The problem of regulation and the reaction of the regulator to varying resistive loads are discussed in Chapter V. Also discussed are the nonlinearities of the regulator and the difficulties encountered in attempting to model such a system for purposes of analysis.

Following the analysis of a single regulator, Chapter VI presents an investigation of the complete power system consisting of eighteen regulators in parallel and under the control of a power sharing circuit. To study the parallel arrangement, a feedback diagram is developed and the system output voltage and individual regulator currents are formulated in terms of load resistance, distribution line resistances and two intrinsic properties of the individual regulators: the output resistance and the no-load output voltage.

Chapter VII contains a presentation of some of the results obtainable from the computer program model. The results are in the form of graphs displaying changes in one or more variables for a variety of input voltage and load resistance conditions. The conclusions given in this chapter summarize the work done, the results obtained, and suggest areas that could be investigated further.

II. SYNOPTIC VIEW

A discussion of the principles of operation of the regulator of the CBRM will be presented in this chapter and a detailed analysis of each part of the regulator will be presented in Chapter III. A simplified block diagram of the regulator, showing the major blocks is shown in Figure 2-1.

The principle function of the regulator is to take energy from one voltage supply whose voltage may be any value over a wide range (bank of solar cells) and use this energy to maintain an output voltage at a relatively fixed value. Since it is possible for the output voltage of the source supply to be less than the required regulated output, it is necessary to temporarily store this energy in the transition from input to output. The temporary storage element used is an inductor called the charging inductor located in the lower right-hand block of Figure 2-1 and the energy is temporarily stored in the magnetic field of this inductor. The charging inductor is an integral part of an averaging filter which is also included in the same block of Figure 2-1. The energy from the inductor is transferred to large capacitors in the filter. The energy transferred from the supply source is equal to the energy supplied to the load connected to the output terminals plus a small amount lost in the switch and filter.

When the switch in Figure 2-1 is closed, energy is transferred from the input supply to the magnetic field of the inductor and when the

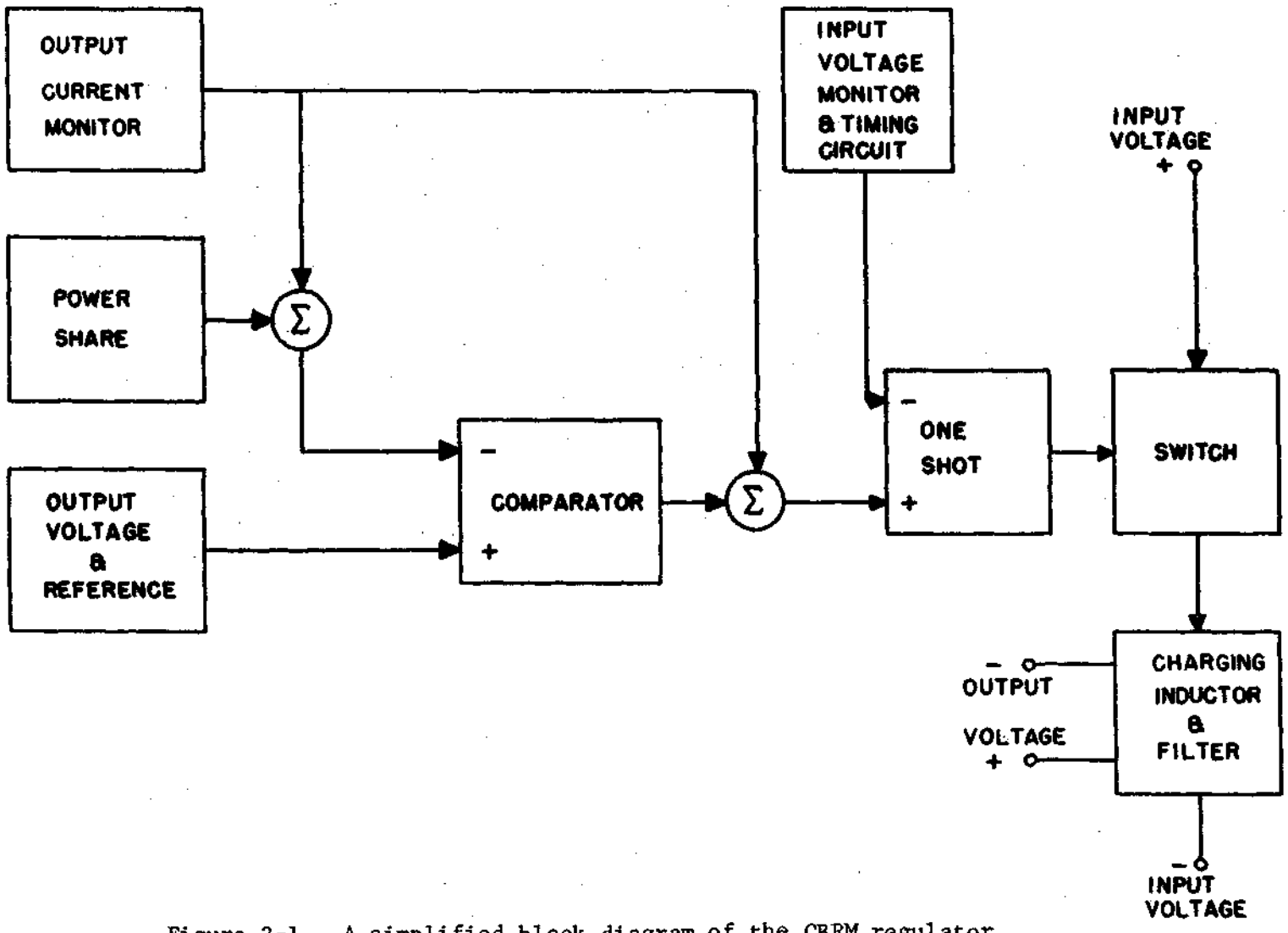

Figure 2-1. A simplified block diagram of the CBRM regulator.

switch is opened, this energy is transferred to the capacitors and load. Each time the switch closes and opens one increment of energy is transferred from the supply source to the capacitors and load. The size of this increment, which must be dependent on the amount of energy being used in the load, is a function of the switch time and the input voltage. The on time of the switch is controlled by a one-shot multivibrator whose timing is controlled by other blocks in Figure 2-1. If the regulator is operated independently of other regulators, the switch time, in order to maintain constant output voltage, would be dependent only on the input voltage and the difference between the output voltage and required voltage. However, the regulator in Figure 2-1 is designed to operate in parallel with several regulators to supply the total power to the load. So that all regulators furnish approximately the same amount of output power, their output currents are made the same. To accomplish this, the output current of each regulator is monitored and compared to a programmed current developed by a power sharing network. Each comparison produces a feedback signal which influences the timing of each switch to equalize the output currents. The output current monitor and power share blocks perform this function as will be explained later in Chapter VI. The output current monitor is also used to reduce the output voltage as a function of output current to give a characteristic as shown in Figure 2-2. The current monitor has a threshold value at 15.5 amperes that will cut the device down rapidly for overload protection.

In order to understand the basic operation associated with the incremental energy transfer from the input source to the output for the

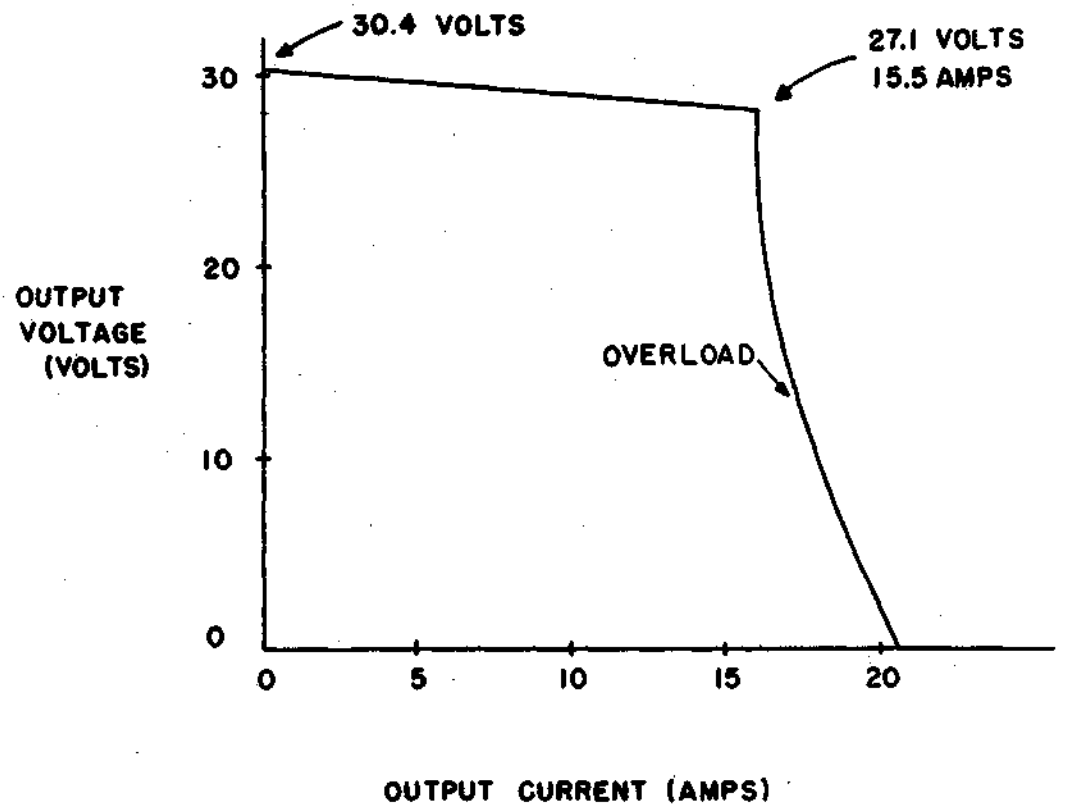

Figure 2-2. The output voltage/output current characteristic.

purpose of voltage regulation, three basic circuits will be discussed. The first circuit has an output voltage that is controllable from zero up to the input voltage depending on the timing of the switch. The second circuit has an output voltage that is controllable from a greater value than the input voltage down to the input voltage, depending on the timing of the switch. The third circuit, has an output voltage that is controllable from a value greater than the input voltage down to zero.

All three circuits will contain two switches, S_1 and S_2, and will be analyzed under periodic operation of these switches. The period of the periodic operation is the time between consecutive closings of S_1. The switch S_1 is assumed to be closed for τ_1 seconds and opened for τ_2 seconds, thus giving a period of τ_1 plus τ_2 seconds. The second switch S_2 is synchronized with S_1 and is opened when S_1 is closed and closed when S_1 is opened. For convenience, a term D has been defined as the duty cycle of S_1 and is the fraction of the period during which S_1 is closed and is given by $D = \tau_1/(\tau_1 + \tau_2)$.

A fourth circuit to be discussed is a modification of the third example and is the actual circuit used in the regulator of the CBRM.

Four Basic Configurations of Output Stages

I. Buck Circuit

The circuit in Figure 2-3 will have an output voltage whose average value will be between zero and V_s depending on the duty cycle of switch S_1. The voltage v(t) in Figure 2-3 is shown in Figure 2-4. A linear analysis of the circuit to the right of switch S_2 reveals that the output voltage will have the same average value as v(t). This

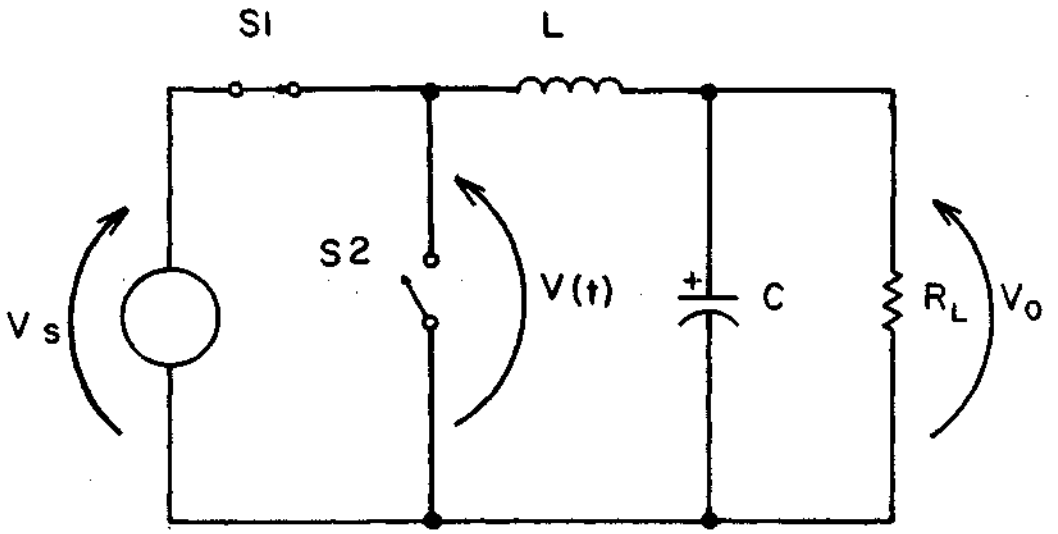

Figure 2-3. The circuit of a Buck type output stage.

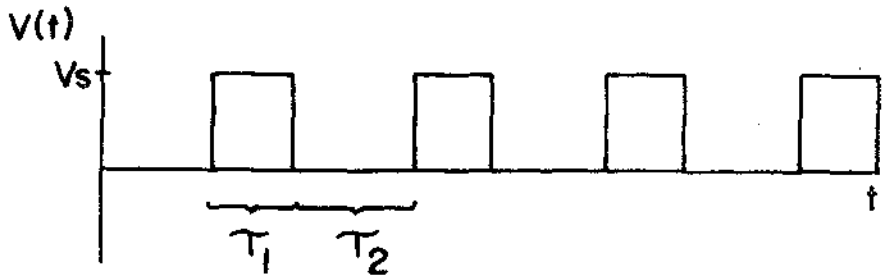

Figure 2-4. The waveform of v(t), the voltage across S2 of Figure 2-3.

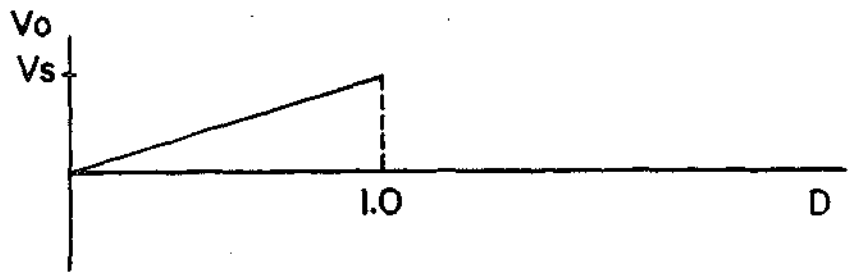

Figure 2-5. The range of possible values for the output voltage V_0 as a function of the duty cycle.

analysis is based on representing v(t) as a Fourier series and realizing that a constant v(t) will produce a constant $v_0(t)$ of the same value. The harmonics of v(t) will also appear in $v_0(t)$; however, they will be attenuated by the low-pass LC filter. The average value of v(t), and $v_0(t)$ is:

$$\langle v(t) \rangle = \langle v_0(t) \rangle = \frac{\tau_1 V_s}{\tau_1 + \tau_2} = DV_s \tag{2-1}$$

and is plotted in Figure 2-5 as a function of D.

II. Boost Circuit

The circuit in Figure 2-6 is commonly known as a Flyback circuit and its output voltage will be between a value greater than V_s and V_s depending on the duty cycle of S_1. In order to solve for the output voltage during steady-state, steady-state conditions are assumed. It is also assumed that during the time that S_1 is closed, the voltage $v_0(t)$ will not change an appreciable amount. Under these conditions the voltage v(t) in Figure 2-6 will have the waveform shown in Figure 2-7. Since the current in L is continuous and periodic, the average value of the voltage across L over one period will be

$$\frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\int_0^T L\,\frac{di(t)}{dt}\,dt = \frac{L}{T}[i(T) - i(0)]. \tag{2-2}$$

Under steady-state conditions the value of the current through the inductor at the end of a period, T, is equal to the value of current through the inductor at the beginning of the period. Thus, by Equation 2-2 the

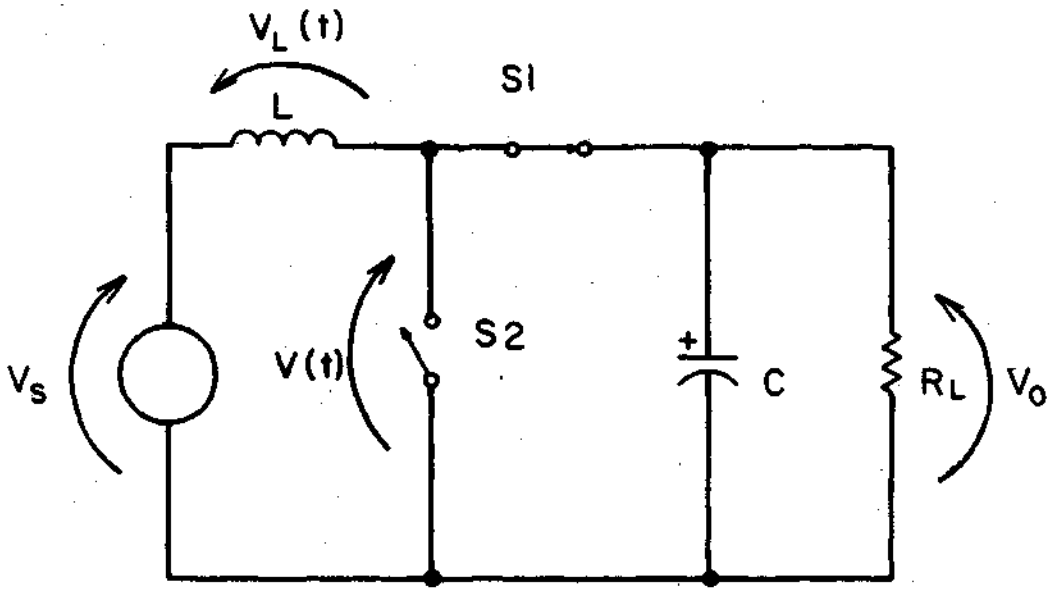

Figure 2-6. The circuit of a Boost or Flyback type output stage.

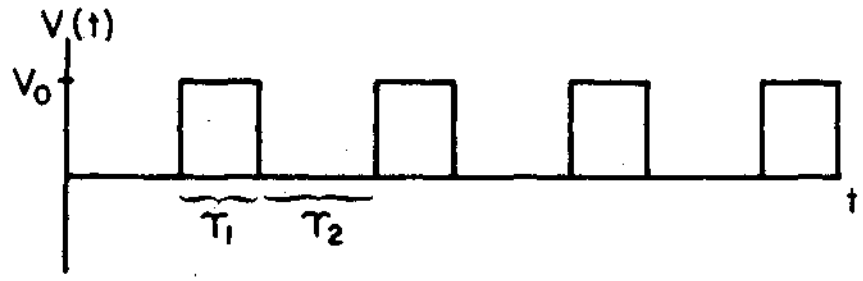

Figure 2-7. The waveform of v(t), the voltage across S2 of Figure 2-6.

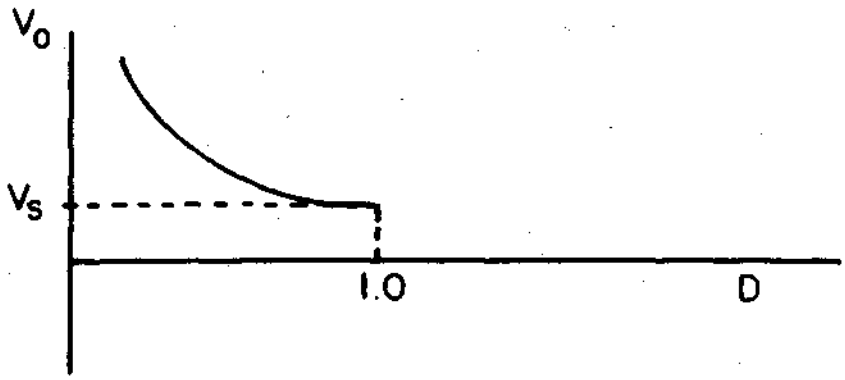

Figure 2-8. The range of possible values for the output voltage V_0 as a function of the duty cycle.

average value of the voltage across the inductor is zero. Solving for the average value of v(t), the voltage across S_2:

$$v(t) = V_s - v_L(t) \tag{2-3}$$

$$\langle v(t) \rangle = \langle V_s \rangle - \langle v_L(t) \rangle \tag{2-4}$$

$$\langle v(t) \rangle = \langle V_s \rangle \tag{2-5}$$

The average value of v(t) in terms of V_0 can be calculated using Figure 2-7:

$$v(t) = \frac{\tau_1 V_0}{\tau_1 + \tau_2} = DV_0 \tag{2-6}$$

Combining the two equations for v(t) and solving for V_0:

$$V_0 = \frac{1}{D} V_s \ . \tag{2-7}$$

V_0 is plotted as a function of D in Figure 2-8.

III. Buck-Boost Circuit

The circuit in Figure 2-9 will have an output voltage whose average value will be between a value greater than the input voltage and zero, depending on the duty cycle of switch S_1. As was done for the Boost configuration, an expression for V_0 as a function of D can be derived for steady-state conditions with a continuous and periodic current through L. Again the average value of v(t), the voltage across the induc-

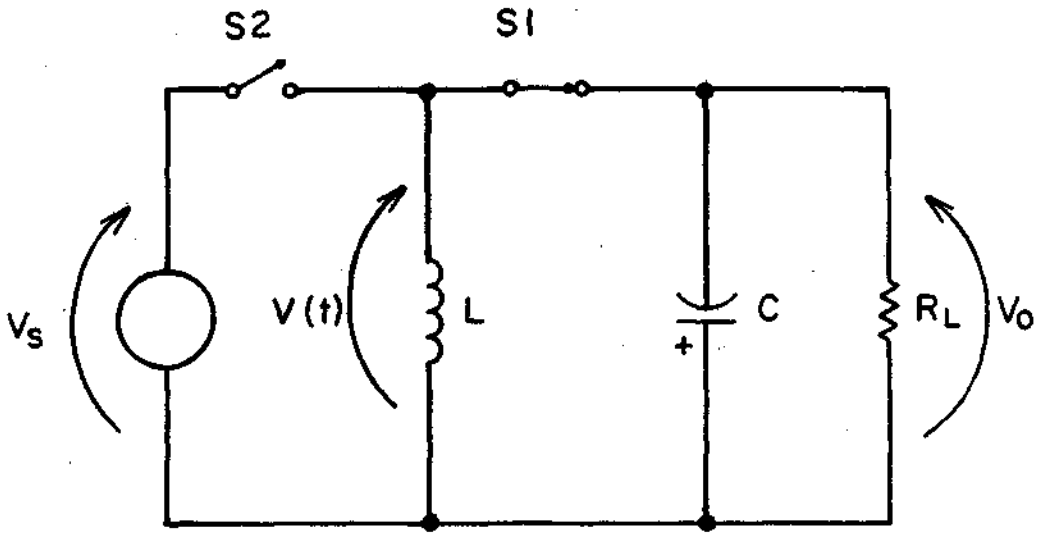

Figure 2-9. The circuit of a Buck-Boost type output stage.

tor is zero. From Figure 2-10 which shows v(t) as a function of time,

$$\langle v(t) \rangle = \frac{\tau_1 V_0 + \tau_2 V_s}{\tau_1 + \tau_2} = 0 \quad . \tag{2-8}$$

Solving for V_0 from this equation yields:

$$DV_0 + (1 - D)V_s = 0 \tag{2-9}$$

$$V_0 = - \frac{1 - D}{D} V_s \quad . \tag{2-10}$$

The possible range of V_0 is shown in Figure 2-11 and as indicated by Equation 2-10 will have negative values.

IV. Modified Buck-Boost Circuit

The output stage used in the CBRM regulator is a modified version of the Buck-Boost configuration just discussed. As shown in Figure 2-12, a segment of time τ_3 (known as dwell time) is introduced in which both switches, S_1 and S_2, will be opened. A drawing of this configuration is given in Figure 2-13 and the waveform for v(t) appears in Figure 2-14.

The average value of v(t) will be zero as discussed for the two previous configurations and with the aid of Figure 2-14 can be expressed as:

$$\langle v(t) \rangle = \frac{\tau_1}{\tau_1 + \tau_2 + \tau_3} V_0 + \frac{\tau_2}{\tau_1 + \tau_2 + \tau_3} V_s = 0 \tag{2-11}$$

$$DV_0 + \frac{\tau_1 + \tau_2 + \tau_3 - \tau_1 - \tau_3}{\tau_1 + \tau_2 + \tau_3} V_s = 0 \tag{2-12}$$

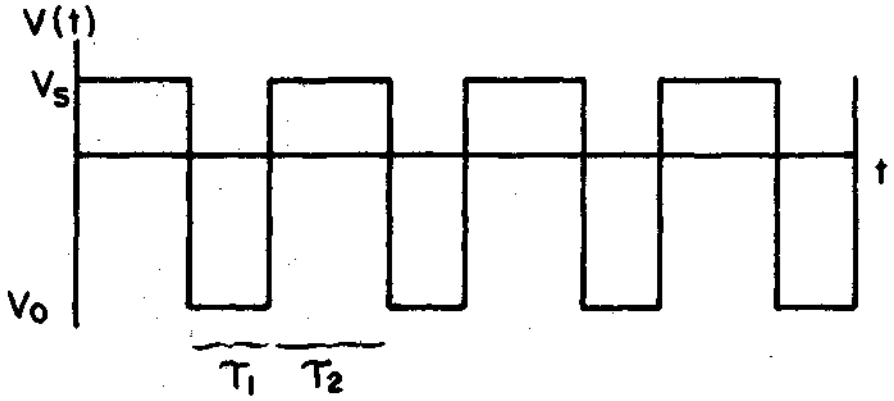

Figure 2-10. The waveform of v(t), the voltage across L of Figure 2-9.

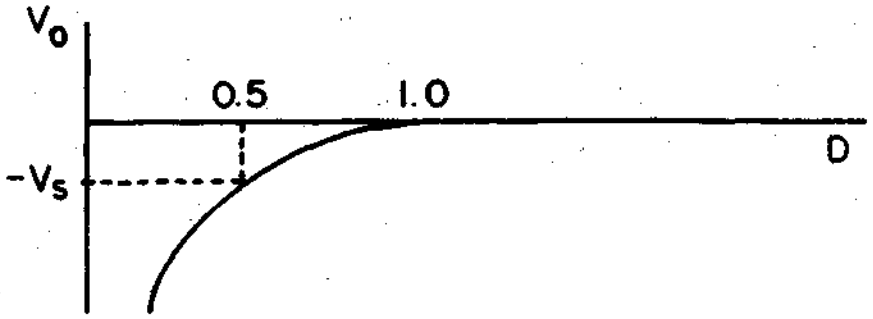

Figure 2-11. The range of possible values for the output voltage V_0 as a function of the duty cycle.

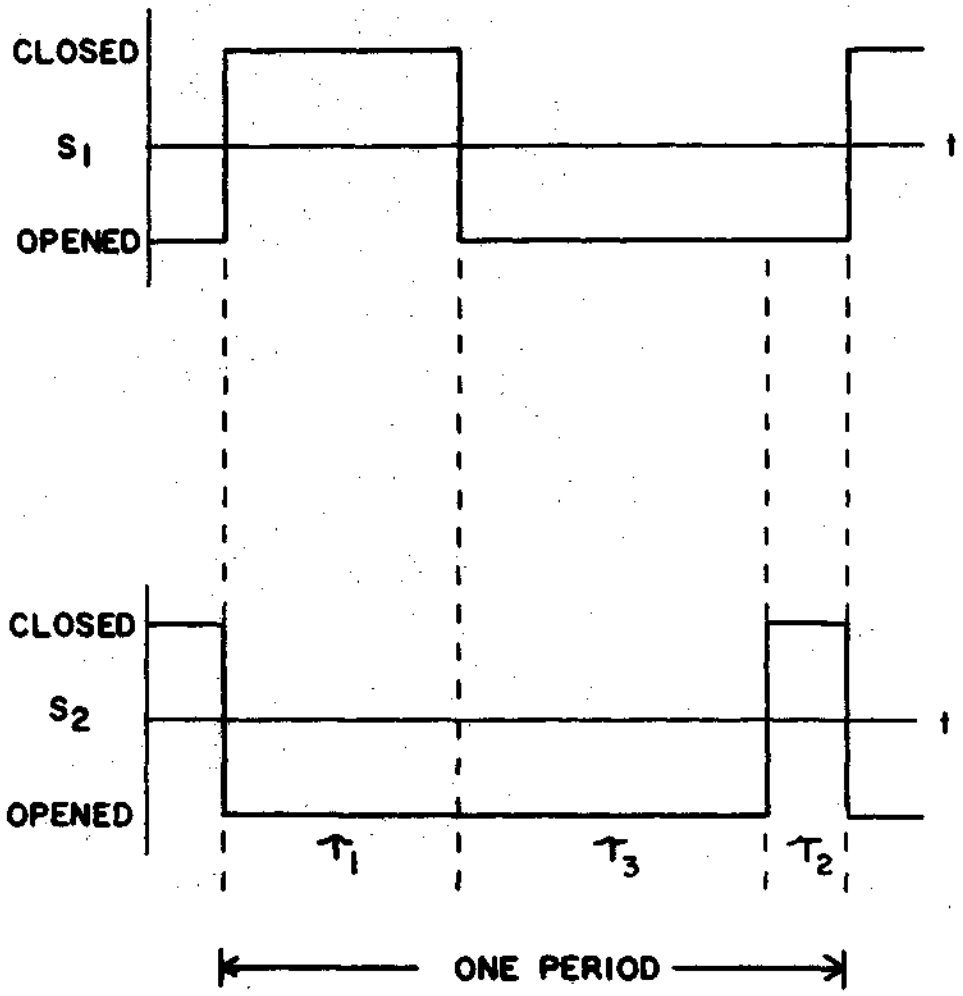

Figure 2-12. A graph of the switch position relationship between S1 and S2 of the Modified Buck-Boost output stage.

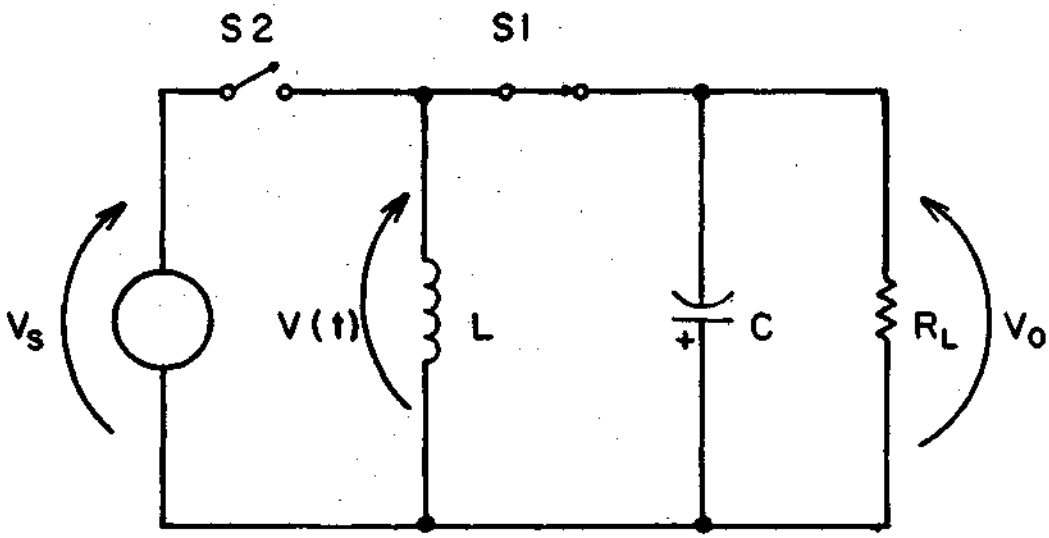

Figure 2-13. The circuit of a Modified Buck-Boost type output stage.

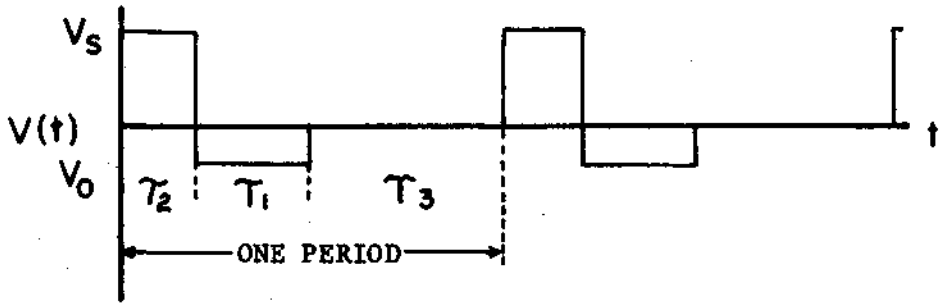

Figure 2-14. The waveform of v(t), the voltage across L of Figure 2-13.

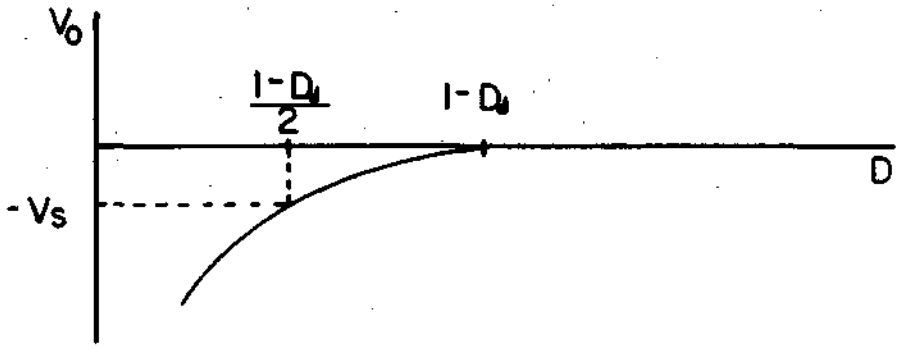

Figure 2-15. The range of possible values for the output voltage V_0 as a function of the duty cycle.

$$DV_0 + (1 - D - D_d)V_s = 0 \tag{2-13}$$

$$V_0 = - \frac{1 - D - D_d}{D} V_s \tag{2-14}$$

where $$D_d = \frac{\tau_3}{\tau_1 + \tau_2 + \tau_3} \tag{2-15}$$

and is the fraction of time when both switches are opened. A plot of V_0 as a function of D for a constant D_d is shown in Figure 2-15.

In the actual circuit of the CBRM regulator, large amounts of current must be switched by S_1 and S_2 and carried by L. To facilitate handling this current, four branches each composed of an S_1, S_2 and L are paralleled and each takes a fourth of the total current. Switch S_1 is a silicon power diode and S_2 is a silicon power transistor. This arrangement is shown in Figure 2-16. For purpose of analysis, the four inductors in parallel can be considered as one with an equivalent value.

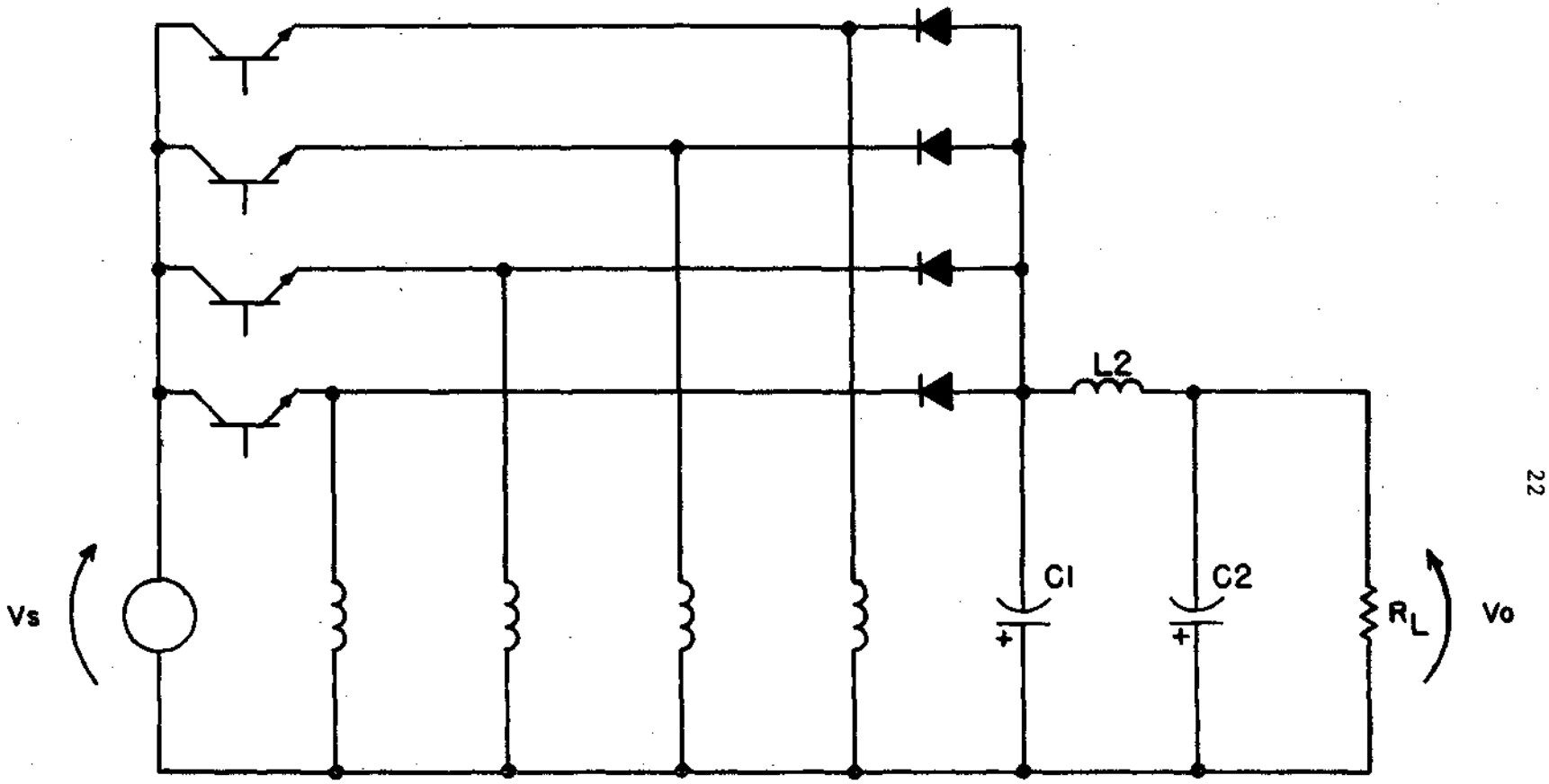

Figure 2-16. A part of the output stage of the CBRM showing the four transistor switches, four charging inductors and four diode switches.

III. MATHEMATICAL DERIVATIONS

Derivation of the mathematical equations governing the operation of the regulator will be developed based on the piece-wise linear behavior of the system. To understand the piecewise-linear behavior, let it be assumed that the regulator is in a normal mode of operation with an output current being delivered to a load. The output voltage is continuously compared with an internal reference voltage and if low-voltage condition is indicated, the one-shot multivibrator is triggered. The on time of the multivibrator is a function of the input voltage and the output current. The output of the multivibrator is used to turn on transistor switches which allow the charging inductor to receive energy from the input source. The amount of energy stored in the inductor is a function of the on time of the multivibrator and the value of the input voltage supply. The higher the input voltage the shorter the time required to store a given amount of energy. Also, since the energy delivered to the load must balance with the energy transferred through the inductor, it is necessary that the on time of the multivibrator increase as a function of the load current. Therefore, the on time of the multivibrator is a decreasing function of the input voltage and an increasing function of the output current. When the multivibrator turns off the transistor switches, the energy in the charging inductor is transferred into the output filter as explained in Chapter II. When the current in the inductor reaches zero, the energy dump from the inductor to filter

is complete and control of the regulator is returned to the comparator. The multivibrator is again automatically triggered as soon as the comparator determines that a low-voltage condition exists. This sequence of events constitutes one cycle of operation of the switching regulator.

During steady-state operation, there is a time interval between the end of the energy dump and the condition necessary for the retriggering of the multivibrator. This is due to the building up of the output voltage by the energy just dumped by the charging inductor, and then waiting for this voltage to decrease. This wait period is usually called dwell, or off, time.

One cycle of operation consists of three distinct time intervals; the inductor charging time, the inductor dumping time, and the dwell time. The operation of each part of the regulator will be analyzed for the three time intervals. The output filter is analyzed first followed by an analysis of the charging inductor. The results of these analyses will then be used to determine the necessary timing equations for satisfactory operation of the regulator.

A. Output Filter Currents

The output filter is shown in Figure 3-1 and is a fourth-order network when the commutating diode is forward biased (dumping time interval) and is a third-order network when the diode is reverse biased (charging and dwell time). The mathematical analysis is divided into two parts depending on the state of the diode. The mode of operation during the time interval when the diode is forward biased will be referred to as mode A and the mode of operation during the time interval when the diode is reverse biased will be referred to as mode B.

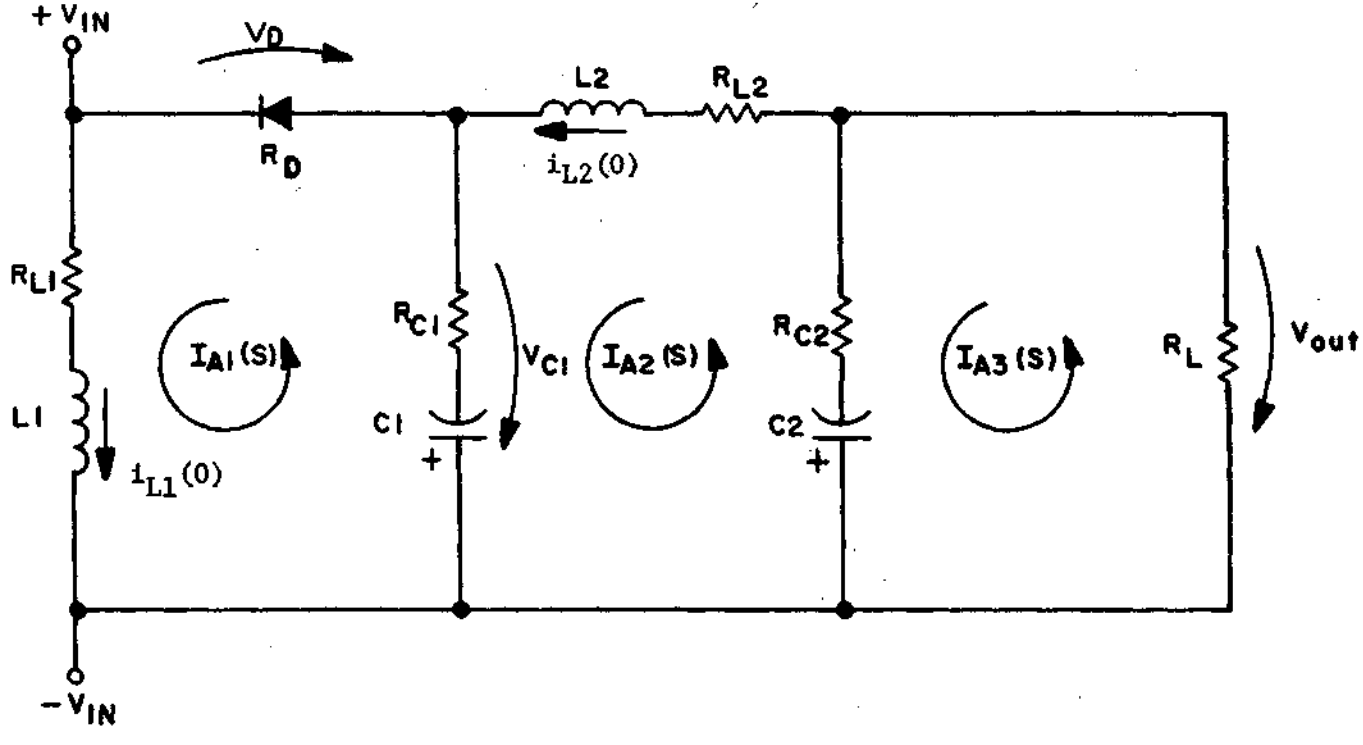

Figure 3-1. The output filter in Mode A.

The equations for the filter currents will now be derived for mode A operation. A matrix equation for the loop currents, in Laplace transform terms, is given on page 27 as Equation 3-1. In the matrix equation and the following analysis (for mode A), the diode is modeled as a small voltage source, V_D, in series with a small resistance. The form of $I_{A1}(S)$, $I_{A2}(S)$, and $I_{A3}(S)$ is:

$$I_A(S) = \frac{-V_D}{R_D + R_{L1} + R_{L2} + R_L} \frac{1}{S} + \frac{a_3S^3 + a_2S^2 + a_1S + a_0}{b_4S^4 + b_3S^3 + b_2S^2 + b_1S + b_0} \quad (3\text{-}2)$$

The derivation of this equation and expressions for the coefficients are given in Appendix A.

The last term of Equation 3-2 has a denominator which can be expanded into two complex conjugate pairs of roots and can be written in the form of:

$$\text{last term} = \frac{R_{A1} \angle \theta_{A1}}{S+\alpha_{A1}-j\omega_{A1}} + \frac{R_{A1} \angle -\theta_{A1}}{S+\alpha_{A1}+j\omega_{A1}} + \frac{R_{A2} \angle \theta_{A2}}{S+\alpha_{A2}-j\omega_{A2}} + \frac{R_{A2} \angle -\theta_{A2}}{S+\alpha_{A2}+j\omega_{A2}} \quad (3\text{-}3)$$

Thus, the time domain expression for the currents will have the form of:

$$\begin{aligned} i_A(t) = {} & 2R_{A1} \exp[-\alpha_{A1}t] \cos(\omega_{A1}t + \theta_{A1}) \\ & + 2R_{A2} \exp[-\alpha_{A2}t] \cos(\omega_{A2}t + \theta_{A2}) \\ & - V_D/(R_D + R_{L1} + R_{L2} + R_L) \quad . \end{aligned} \quad (3\text{-}4)$$

Each parameter in the current equations is defined and discussed in Appendix B.

$$\begin{bmatrix} \left(\frac{1}{SC1} + SL1 + R_{L1} + R_{C1} + R_D\right) & \left(-\frac{1}{SC1} - R_{C1}\right) & 0 \\ \left(-\frac{1}{SC1} - R_{C1}\right) & \left(\frac{1}{SC1} + \frac{1}{SC2} + SL2 + R_{C1} + R_{C2} + R_{L2}\right) & \left(-\frac{1}{SC2} - R_{C2}\right) \\ 0 & \left(-\frac{1}{SC2} - R_{C2}\right) & \left(\frac{1}{SC2} + R_L + R_{C2}\right) \end{bmatrix} \cdot \begin{bmatrix} I_{A1}(S) \\ I_{A2}(S) \\ I_{A3}(S) \end{bmatrix}$$

$$= \begin{bmatrix} L1 \cdot i_{L1}(0) - v_{C1}(0)/S - V_D/S \\ L2 \cdot i_{L2}(0) + v_{C1}(0)/S - v_{C2}(0)/S \\ v_{C2}(0)/S \end{bmatrix} \qquad (3\text{-}1)$$

where $i_{L1}(0)$ is the initial current through L1,

$i_{L2}(0)$ is the initial current through L2,

$v_{C1}(0)$ is the initial voltage across C1,

$v_{C2}(0)$ is the initial voltage across C2, and

V_D is the forward voltage drop across the diode.

When the diode is reverse biased, it is in mode B operation and appears as shown in Figure 3-2. A matrix equation for the loop currents in Laplace transform terms is:

$$\begin{bmatrix} \left(\frac{1}{SC1} + \frac{1}{SC2} + SL2 + R_{C1} + R_{C2} + R_{L2}\right) & \left(-\frac{1}{SC2} - R_{C2}\right) \\ \left(-\frac{1}{SC2} - R_{C2}\right) & \left(\frac{1}{SC2} + R_{C2} + R_L\right) \end{bmatrix} \cdot \begin{bmatrix} I_{B2}(S) \\ I_{B3}(S) \end{bmatrix}$$

$$= \begin{bmatrix} L2 \cdot i_{L2}(0) + v_{C1}(0)/S - v_{C2}(0)/S \\ v_{C2}(0)/S \end{bmatrix} \qquad (3\text{-}5)$$

where $i_{L2}(0)$ is the initial current through L2,

$v_{C1}(0)$ is the initial voltage across C1, and

$v_{C2}(0)$ is the initial voltage across C2.

The form for $I_{B2}(S)$ and $I_{B3}(S)$ then will be:

$$I_B(S) = \frac{c_2S^2 + c_1S + c_0}{d_3S^3 + d_2S^2 + d_1S + d_0} \qquad (3\text{-}6)$$

Equation 3-6 has a denominator which can be expanded into a complex conjugate pair and one real root and can be written in the form of:

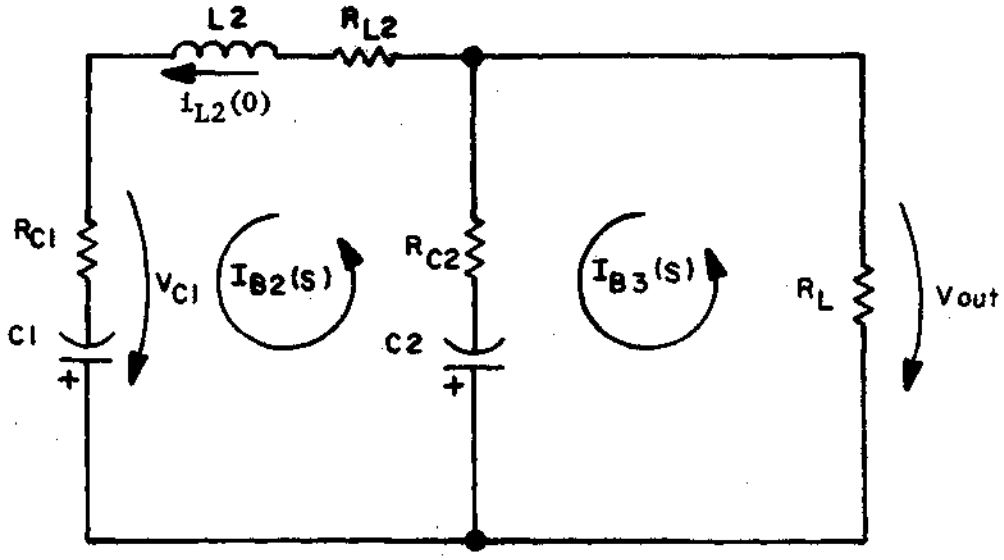

Figure 3-2. The output filter in Mode B.

$$I_B(S) = \frac{R_{B1} \angle \theta_{B1}}{S+\alpha_{B1}-j\omega_{B1}} + \frac{R_{B1} \angle -\theta_{B1}}{S+\alpha_{B1}+j\omega_{B1}} + \frac{R_{B2}}{S+\alpha_{B2}} \tag{3-7}$$

Thus, the time domain expression for the currents will have the form of:

$$i_B(t) = 2R_{B1} \exp[-\alpha_{B1}t] \cos(\omega_{B1}t + \theta_{B1}) + R_{B2} \exp[-\alpha_{B2}t] \tag{3-8}$$

B. Model of Charging Inductor

If the charging inductor, L1, is ideal and the voltage across it is a constant, then the current through it is a linear function of time and is as follows:

$$i(t) = \frac{1}{L1}\int_0^t V_L \, dt \tag{3-9}$$

$$i(t) = \frac{V_L \, t}{L1} \tag{3-10}$$

where V_L is the voltage across the inductor.

However, for large currents, the inductor's value will be a function of the current through it. Under this condition, the current through the charging inductor will still be a function of time but not a linear one, and can be expressed as:

$$i(t) = \int_0^t \frac{V_L}{L1(i)} \, dt \tag{3-11}$$

Since the charging inductor's value does vary with current, it is necessary to model the inductor so that this variation is accounted for. Each charging inductor in the CBRM power supply has a value of inductance of approximately 200 μH when operated well below saturation.

The voltage across L1 can be expressed as:

$$V_L = \frac{d(i(t)\ L1(i))}{dt} \tag{3-12}$$

and holds for any set of time and current values when the proper value of L1 is used. If a very small change is taken in time, L1(i) will be a near constant. Thus:

$$V_L \cong L1(i)\ \frac{\Delta i(t)}{\Delta t} \tag{3-13}$$

The smaller the Δt, the greater the accuracy of this equation. Solving for the change in current:

$$\Delta i(t) = \frac{V_L \Delta t}{L1(i)} \quad . \tag{3-14}$$

This equation will give the increase in current through the inductor for a small increase in time when the inductor's value is known in the range of operation.

Equation 3-14 states that for fixed increments of time, Δt, the increments of current, Δi, get larger as L1(i) decreases. Figure 3-3, drawn from measurements on the actual CBRM regulator, shows the results

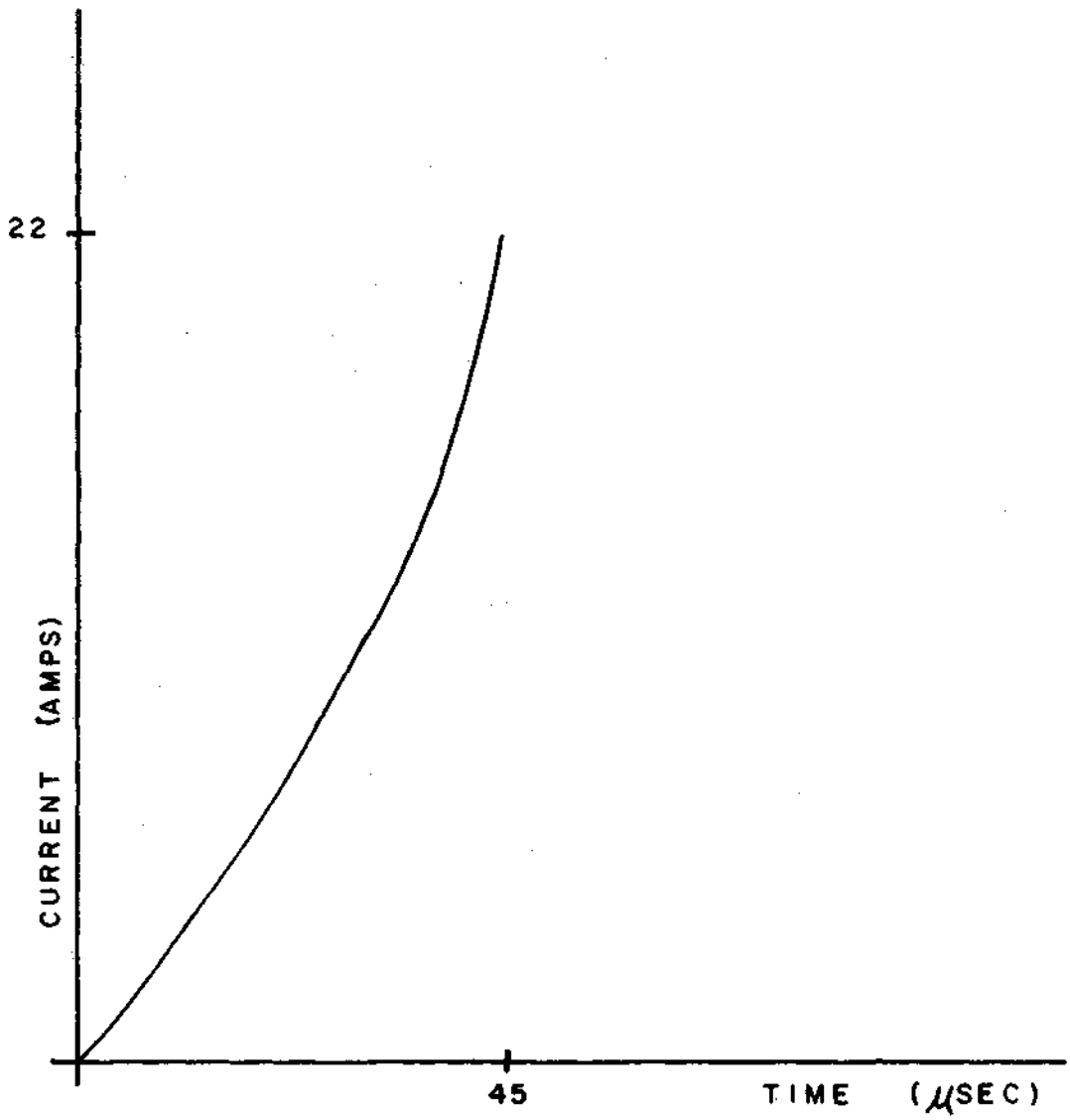

Figure 3-3. A typical charging current curve.

of such action. The input voltage and load current were 60.3 volts and 14.6 amperes, respectively.

It can be seen by Equation 3-14 that the inductance for any value of current is equal to the applied voltage divided by the slope of the current curve at the operating point.

$$L1(i) = \frac{V_L}{\Delta i(t)/\Delta t} \tag{3-15}$$

From measurements on the regulator system, it was calculated that the value of the inductance at two amperes is approximately 200 μH and at twenty amperes the value is approximately 100 μH.

One method of determining the current through the inductor is to use Equation 3-14 and represent L1(i) empirically as:

$$L1(i) = 200\ \mu H - K1(i)^{K2} \tag{3-16}$$

This equation was chosen because it generates values of L1 close to actual values and holds for all i within the range of operation. K1 and K2 are selected constants used to make the equation approximate the actual inductor. Values used for K1 and K2 that gave good results were $0.70(10)^{-6}$ and 1.08, respectively.

An iterative process will now be developed that will relate a value of current through the inductor, L1, to a given fraction of the total time for which a constant voltage is applied across the inductor. Let the total time be T and the applied voltage be V_L. The time T is divided into small segments Δt. Beginning with an initial current of

zero, L1(i) is calculated by Equation 3-16 and used in Equation 3-14 to determine the amount of increase in current, Δi, due to an increase in time Δt. Now using the new value of current, another value of L1(i) is calculated and used to calculate the latest increase in current due to another increase in time. This procedure is continued until the sum of the Δt's equals T, each time using the sum of the Δi's to determine L1(i). This process yields very satisfactory results if Δt is T/20 or smaller.

C. Dwell Time

Whenever the voltage at the input of the output filter is sufficiently high, the one-shot multivibrator should stay off. This off time is called dwell time. Looking at the diagram of the comparator circuit in Figure 3-4, which turns the one-shot on, the voltage equation for its difference-mode input can be written:

$$V_a = \frac{15\ R3 - 7.5K\ V_{C1}}{7.5K + R3} - V_{CURNT} \qquad (3\text{-}17)$$

where V_{C1} is the voltage across the filter capacitor C1, and V_{CURNT} is the voltage at the inverting input of IC2 produced by the output current monitor. The transition of V_a from a negative value to a positive value will cause the comparator's output to go from negative to positive thereby turning the one-shot on.

In determining the dwell time, the question to be answered is "How long does it take for the first capacitor, C1, in the output filter to discharge to a value that would require the one-shot to come on again?"

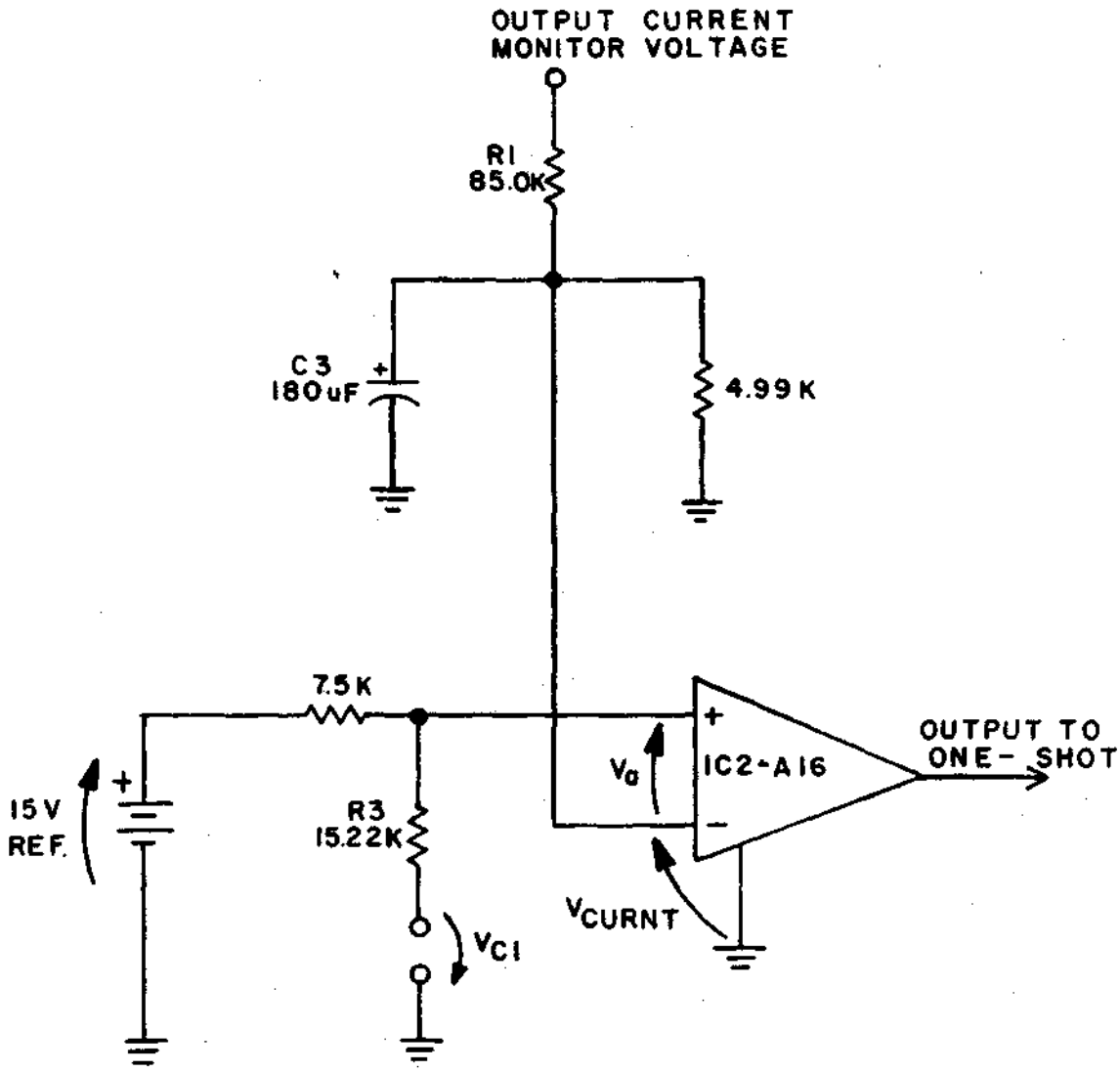

Figure 3-4. The comparator circuit used to determine the dwell time.

V_{C1} has a waveform similar to that shown in Figure 3-5. The exact amplitudes and times are functions of the input voltage and the load current.

Let the value of V_{C1} at the end of the dump time, which will be discussed later, be called $V_{C1\alpha}$ and let the value of V_{C1} that makes V_a go from a negative value to a positive value ($V_a = 0^+$) be called $V_{C1\beta}$. Then the decrease in V_{C1} during the dwell time will be:

$$\Delta V_{C1} = V_{C1\alpha} - V_{C1\beta} \tag{3-18}$$

To develop an expression for the dwell time, another equation for ΔV_{C1} can be used if the current being discharged by C1 is considered a constant. Due to the large value of capacitance and short dwell time, this is a good approximation. Therefore representing dwell time by T_D:

$$\Delta V_{C1} = \frac{1}{C1}\int_{t}^{t+T_D} I_{B2}\, dt \tag{3-19}$$

$$\Delta V_{C1} = \frac{I_{B2}\, T_D}{C1} \tag{3-20}$$

Combining Equations 3-18 and 3-20 and solving for $V_{C1\beta}$, the voltage for which V_a equals 0^+ yields:

$$V_{C1\beta} = V_{C1\alpha} - \frac{I_{B2}\, T_D}{C1} \tag{3-21}$$

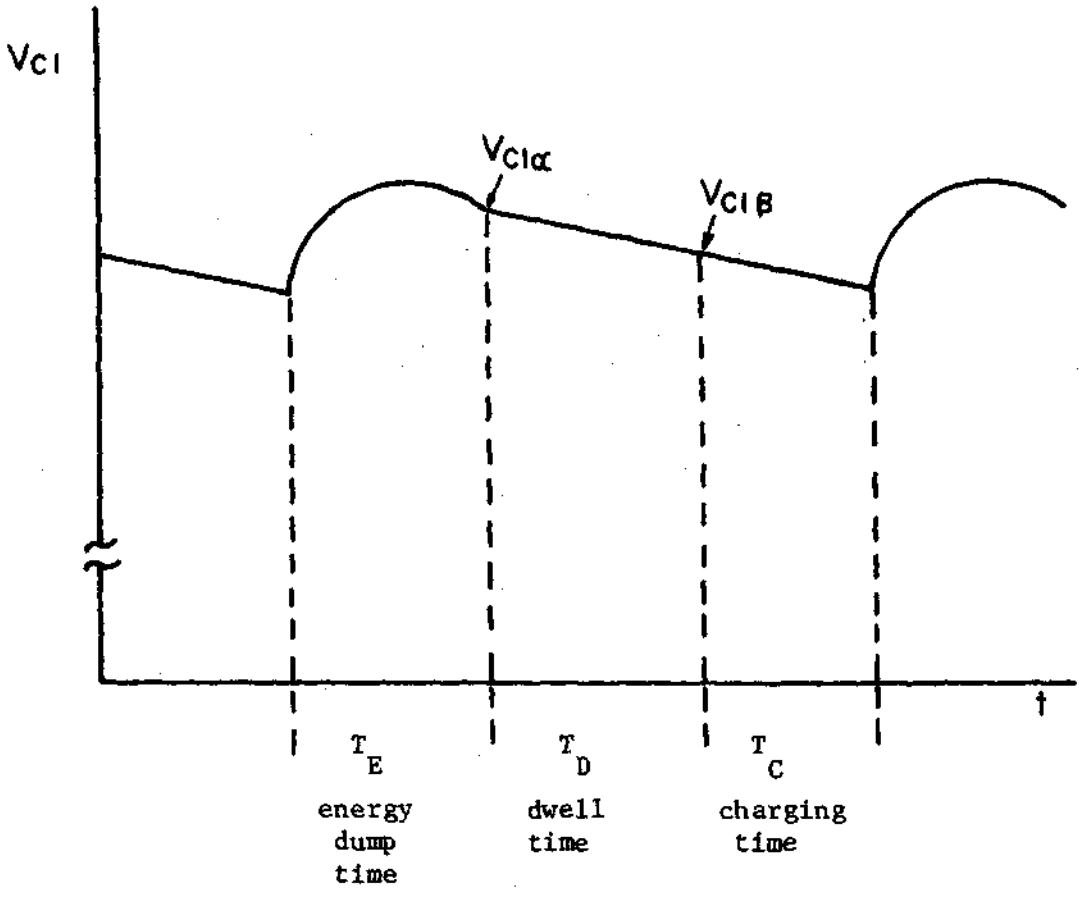

Figure 3-5. A typical waveform of V_{C1}, the voltage across C1.

Using this value of V_{C1} in Equation 3-17 and setting $V_a = 0$ and solving for the dwell time, T_D, yields:

$$T_D = \left[\frac{V_{CURNT}\ (7.5K + R3) - 15\ R3}{7.5K} + V_{C1\alpha}\right]\frac{C1}{I_{B2}} . \qquad (3\text{-}22)$$

Thus, when V_{CURNT}, the voltage at the inverting terminal, $V_{C1\alpha}$, the voltage across C1 at the end of the dump time, and I_{B2}, the current in loop two of the output filter, are known, T_D can be calculated. V_{CURNT} can be determined through an analysis of the RC circuit connected to the inverting input terminal.

D. Charging Time

The charging time is the length of time that the one-shot multivibrator must stay on. The one-shot shown in Figure 3-6 is normally off with -15 volts at the output. Under this condition there is approximately -0.6 volt at the inverting input of IC1 due to CR8 being forward biased and there is approximately -1.7 volts at the noninverting input due to the R18, R23 voltage divider network (CR10 is forward biased and CR6 is reverse biased). The one-shot remains in this stable condition until the current in the charging inductor is zero and the output of the comparator goes positive. When this happens, the noninverting input of IC1 goes positive with respect to the inverting input, the one-shot is turned on, and the output of IC1 goes to 15 volts positive. There will then be current through the charging inductor and when it is detected, the output of IC2 will be drawn to ground potential prohibiting the comparator from having control of the one-shot until the inductor has been charged and completely discharged into the filter. With the comparator's output

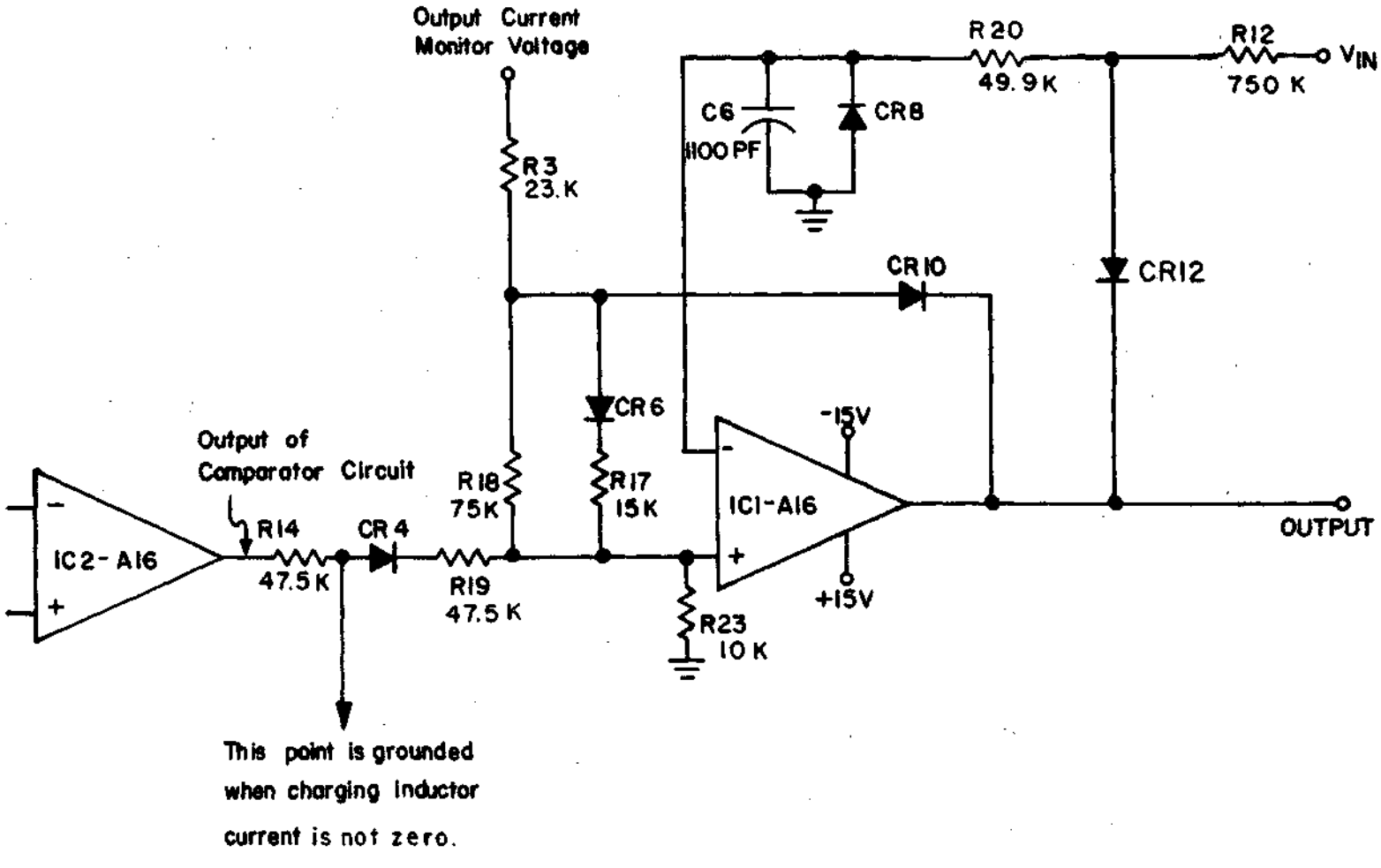

Figure 3-6. The one-shot multivibrator used to develop the on-time of the switching transistors.

grounded, there is a positive voltage on the noninverting input of IC1 from the current monitor which is proportional to the output current. Since CR12 is now reverse biased, C6 will begin to charge. The time interval it takes for the voltage at the inverting input to just exceed that at the noninverting input is the on-time for the switching transistors and charging time for L1, and will be referred to as T_C. At the end of this time, the one-shot will turn off and wait for the next turn-on command.

An expression for T_C in equation form can be developed as follows. First, an equivalent circuit for the input to the 709 operational amplifier, IC1, and the charging path for C6 is modeled in Figure 3-7 in which the input resistance to IC1 has been named R21. Solving for the time required to charge C6 to the value that makes the voltage across R21 equals zero will yield:

$$T_C = \frac{(R12 + R20)(R21 + R22)C6}{R12 + R20 + R21 + R22} \ln \left[\frac{\frac{R12 + R20}{R21 + R22}(V_1 + 0.6) + V_{in} + 0.6}{V_{in} - V_1} \right] \tag{3-23}$$

where $(R3 + R17 \| R18) \| R23$ has been named R22, V_{in} is the input voltage and

$$V_1 = \frac{R23\ (0.9\ I_{B2})}{R23 + R3 + R17 \| R18} . \tag{3-24}$$

$$V_1 \simeq 0.2\ I_{B2} \tag{3-25}$$

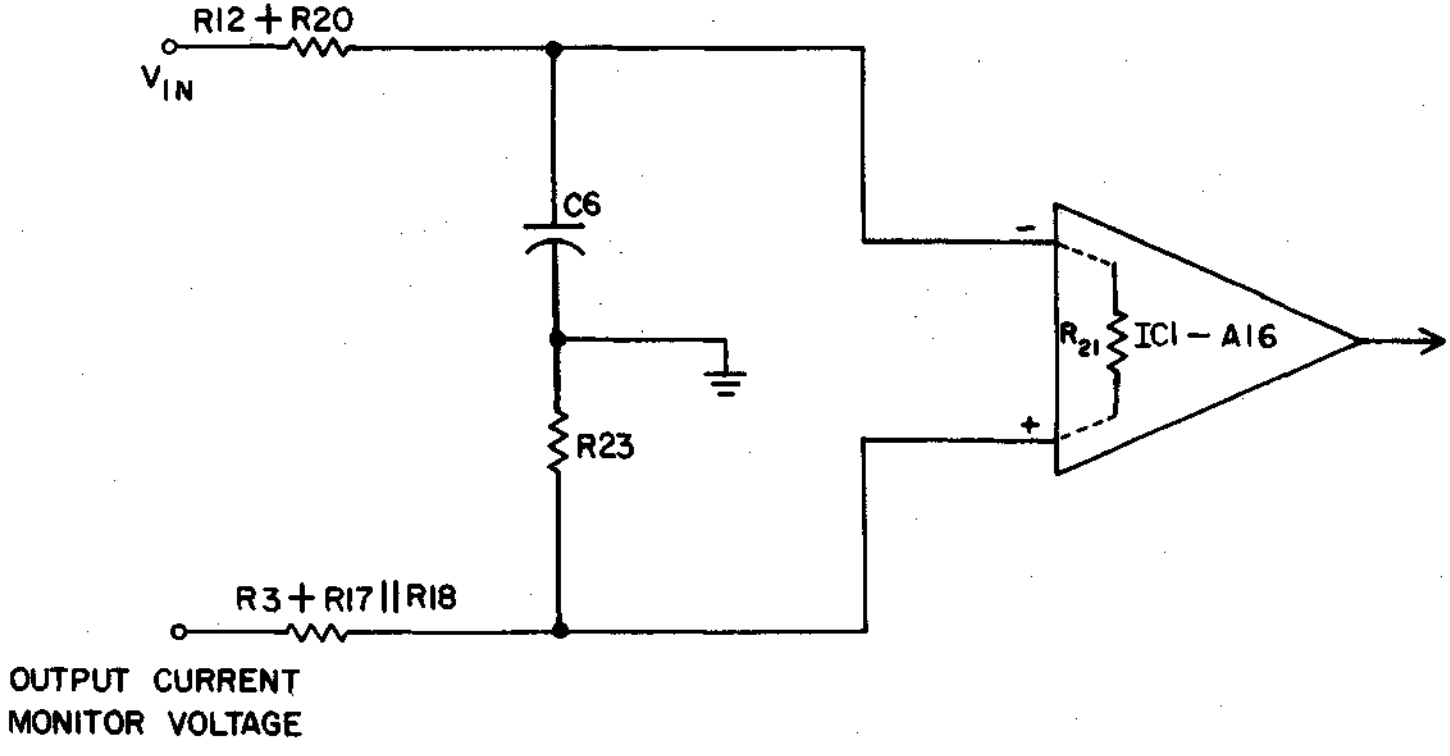

Figure 3-7. An equivalent circuit of the one-shot multivibrator circuit shown in Figure 3-6 when it is in the on state. R21 represents the internal resistance of the operational amplifier.

The voltage, 0.9 I_{B2}, in Equation 3-24 is the voltage appearing at the output-current-monitor voltage terminal shown in Figures 3-6 and 3-7 and is developed as follows. The current in the second loop of the output filter is monitored by a transductor which controls an oscillator. The output of the oscillator is rectified and filtered and produces 0.1 volt per ampere of current. This signal is amplified by a factor of nine and then appears at the output-current-monitor voltage terminal.

Note that if the input resistance, R21, is infinite, the equation for T_C reduces to

$$T_C = (R12 + R20)C6 \ln\left[\frac{V_{in} + 0.6}{V_{in} - V_1}\right] \quad . \tag{3-26}$$

But such is not the case. Typical input resistance for a 709 amplifier is 400 KΩ and can be as low as 150 KΩ. This large but noninfinite value must be considered as an important factor because R12 is in the 600 KΩ to 900 KΩ range.

E. Energy Dump Time

The last interval of time to be determined is that needed for the charging inductor to dump. This energy dump time is called T_E and will be found with the aid of Figure 3-8 which shows only the input branch of the output filter. Due to the relative values of the filter components, most of the current being discharged by L1 is conducted by the input branch. As shown, this branch contains a resistor, R_{C1}, to represent the small effective resistance and an inductor, L_{C1}, to represent the effective inductance of C1.

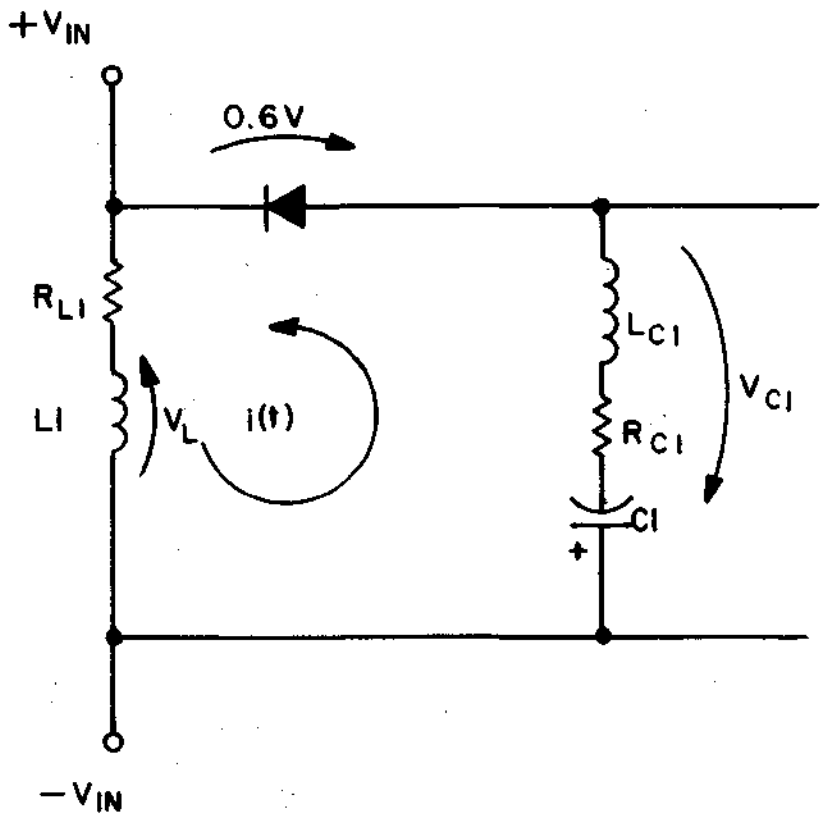

Figure 3-8. The input circuitry of the output filter stage; used to determine the dump time for inductor L1.

It was developed in section B covering the charging inductor, and indicated by Equation 3-14, that the amount of change in current through the inductor for a constant applied voltage, is a function of the length of application time. The voltage across the inductor in the present circumstances will be $-(V_{C1} + 0.6)$ volts and will not be constant throughout the dumping interval due to a small change in V_{C1}; however, this does not affect the validity of the equation. Therefore, the change in current for a small change in time will be:

$$\Delta i(t) = - \frac{(V_{C1} + 0.6)\Delta t}{L1(i)} . \qquad (3\text{-}27)$$

Solving for Δt:

$$\Delta t = - \frac{L1(i)\ \Delta i(t)}{V_{C1} + 0.6} \qquad (3\text{-}28)$$

A suitable $\Delta i(t)$ can be chosen by dividing the initial value of the dumping current, which was the final value of the charging current and will be known, into small segments.

In a manner similar to that used in determining the charging current, the dump time can be found by using an iterative process. After determining a $\Delta i(t)$, Equation 3-16 can be used to calculate L1(i) for the peak value of the charging current. Using this L1(i), a Δt can be calculated by Equation 3-28. An expression for V_{C1} during this time will be developed later. Adding $\Delta i(t)$, a negative number, to the init-

ial current will give the remaining current which is used to calculate the next Δt. Each time through the iterative process, the remaining current through the inductor is determined and used to calculate a new value for L1(i) which in turn is used to calculate a new Δt. When the current has been incremented down to zero the sum of the Δt's will be the total dump time, T_E.

The voltage, V_{C1}, across the branch containing C1 can now be calculated for the interval T_E. This voltage will be made up of a large constant voltage plus a small ripple voltage. Although its name does not explicitly indicate it, V_{C1} will be a function of time and as shown in Figure 3-9 can be expressed as:

$$V_{C1} = v_{C1}(t) + R_{C1}[4\ i(t) - i_{A2}(t)] + V_{L_{C1}} \tag{3-29}$$

where: $v_{C1}(t)$ is the voltage across C1 only,

$i(t)$ is the current dumped by each charging inductor, and

$i_{A2}(t)$ is the current in the second loop of the filter.

Since most of the current being dumped goes only into the branch containing C1 and since the voltage across this branch as well as the output voltage is a near constant, $i_{A2}(t)$ changes very little and will be considered a constant named I_{A2}.

The total current being dumped is four times i(t) and equal to:

$$4i(t) = 4(mt + I_p) = Mt + 4\ I_p \tag{3-30}$$

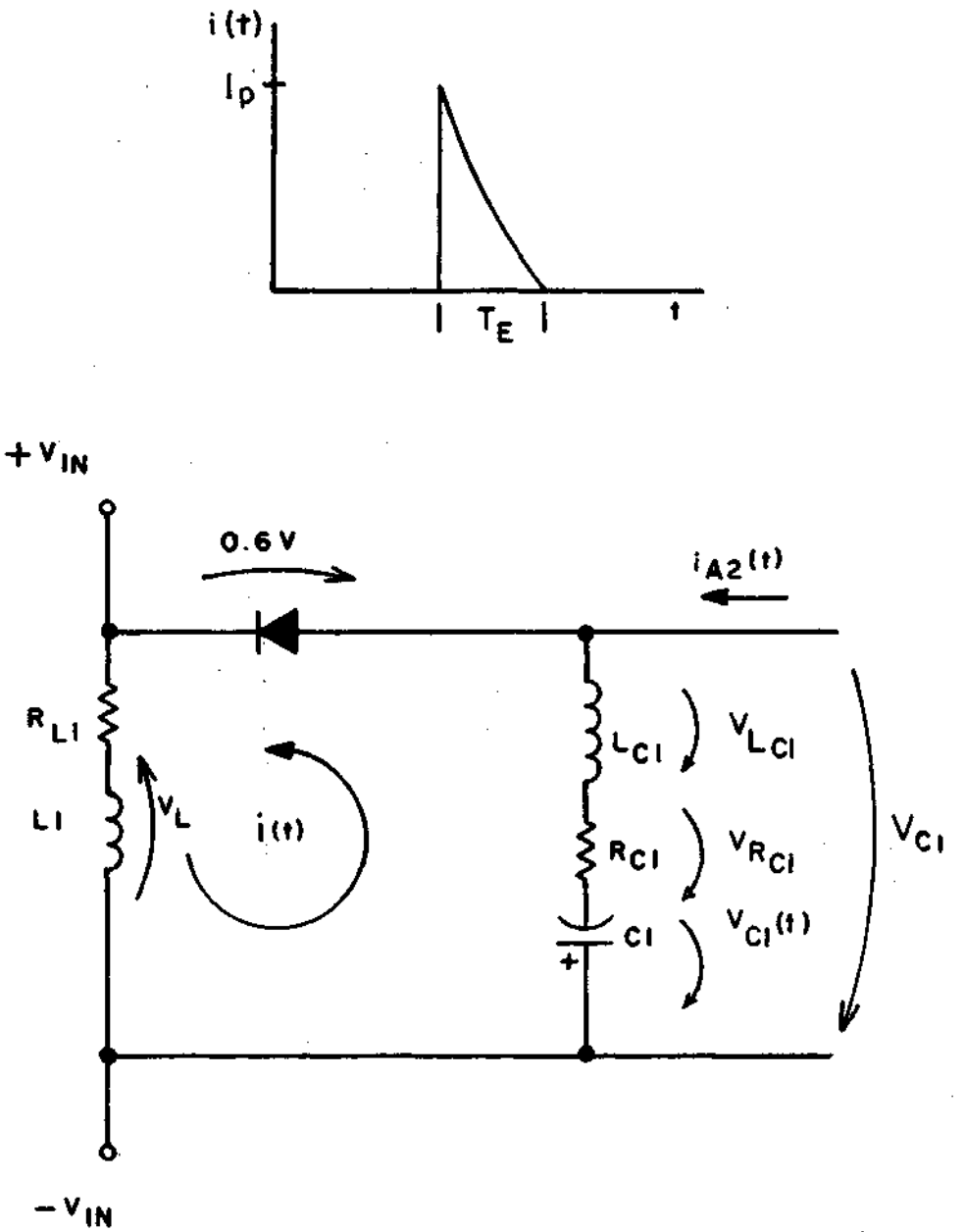

Figure 3-9. The circuit used in determining V_{C1} along with the waveform of the dump current of one inductor.

where m is the slope of i(t) in amperes per second and I_p is the peak value of i(t) at $t = 0^+$.

Considering the slope a constant, $v_{C1}(t)$ can be written as:

$$v_{C1}(t) = \frac{1}{C1}\int_0^t [Mt + 4\ I_p - I_{A2}]dt + v_{C1}(0^+) \qquad (3\text{-}31)$$

where $v_{C1}(0^+)$ is the initial voltage across C1.

Evaluating the integral yields:

$$v_{C1}(t) = \frac{1}{C1}\left[\frac{M}{2}\,t^2 + (4\ I_p - I_{A2})t\right] + v_{C1}(0^+) \qquad (3\text{-}32)$$

While M is not actually a constant it is near so and an expression for it can be found in the interative process developed to calculate T_E. In that process, a $\Delta i(t)$ and Δt were found as the charging inductor dumped. Since four such inductors are present:

$$M = \frac{4\ \Delta i(t)}{\Delta t} \quad . \qquad (3\text{-}33)$$

Thus in the process of calculating the dump time T_E, V_{C1} can be calculated. Each time a Δt is determined, it is used with the $\Delta i(t)$ to compute V_{C1} by the following:

$$V_{C1} = \frac{1}{C1}\left[2 \frac{\Delta i(t)}{\Delta t} t^2 + (4 I_p - I_{A2})t \right] + v_{C1}(0^+)$$

$$+ R_{C1} [4 i(t) - I_{A2}] + V_{L_{C1}} . \qquad (3\text{-}34)$$

Before the above equation can be applied, $V_{L_{C1}}$ must be known. Consider Figure 3-10 which approximates the current flowing through one transistor switch, the current being dumped into C1 from one charging inductor, and the current in one charging inductor. The time interval τ_{off} is the turn-off time of the transistor switches and has been exaggerated in the drawing. For the transistor switches in the regulator, τ_{off} will be less than or near one microsecond depending on the base drive and the amount of current being switched.

As long as the switches are in the process of closing, the total voltage across L_{C1} is :

$$V_{L_{C1}} = L_{C1} \frac{4 I_p}{\tau_{off}} \qquad (3\text{-}35)$$

if a constant slope for the current is assumed. During T_E, shown in Figure 3-10, the total voltage across L_{C1} is equal to:

$$V_{L_{C1}} = L_{C1} \frac{d(4 i(t))}{dt} \qquad (3\text{-}36)$$

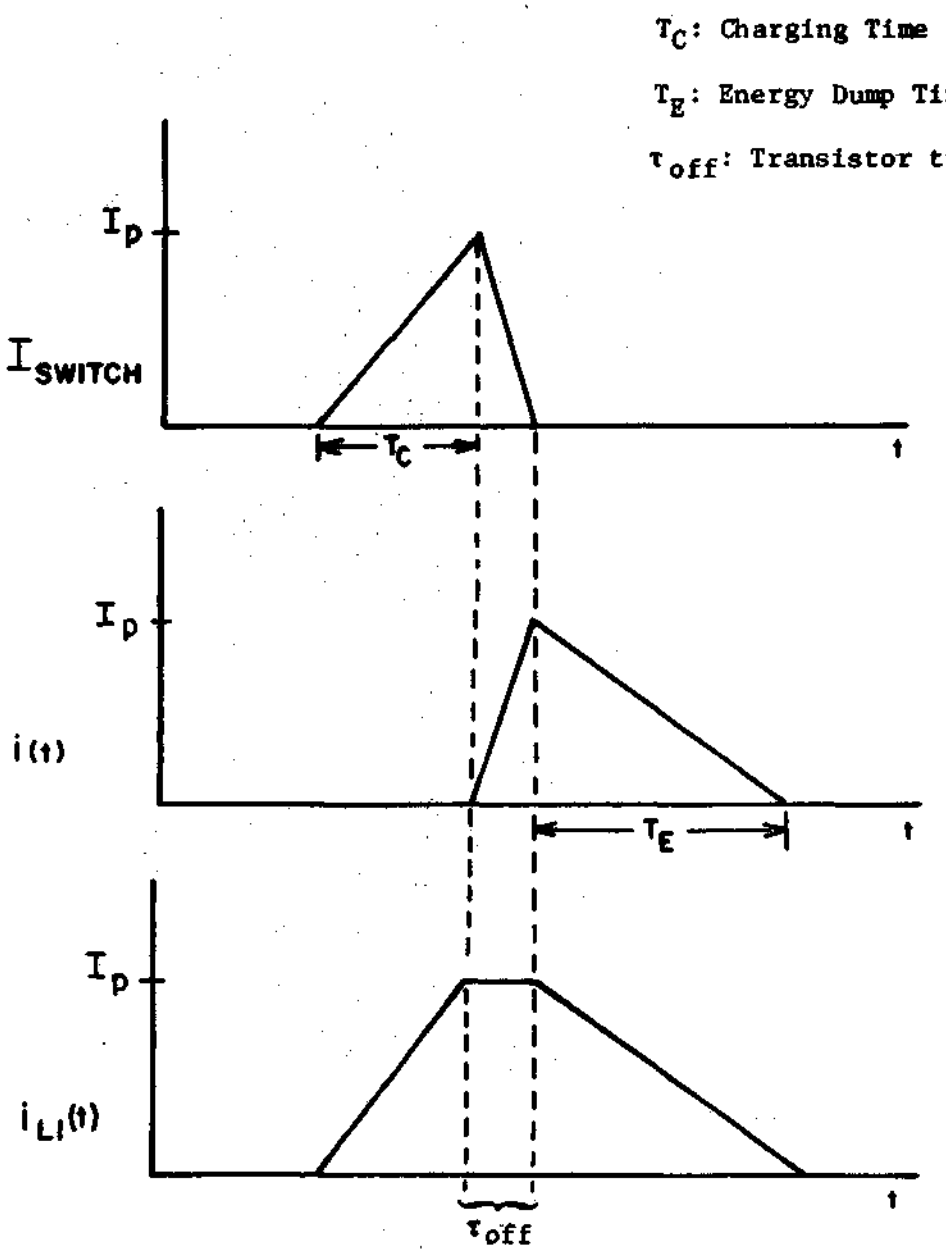

Figure 3-10. Current waveforms associated with charging and discharging L1. The time internal τ_{off} has been exaggerated.

$$V_{L_{C1}} \simeq 4\ L_{C1}\ \frac{\Delta i(t)}{\Delta t} \qquad (3\text{-}37)$$

and will have a negative value. In the computer program, Equation 3-35 will be used to calculate $V_{L_{C1}}$ during the first microsecond after the charging time, T_C, and Equation 3-37 will be used thereafter.

Using the equations developed in this chapter, it is now possible to construct a computer program model of the CBRM. The output voltage will be as shown previously in Figure 2-2 on page 7, and can be expressed as:

$$V_{OUT} = 30.4 - 0.213\ I_{OUT} \qquad (3\text{-}38)$$

where 30.4 is the Thevenin voltage (no-load voltage), 0.213 is the Thevenin resistance (effective dc output resistance), and I_{OUT} is the output current.

IV. COMPUTER PROGRAM MODEL

This chapter contains the listing of a computer program model of the CBRM regulator which was developed using the mathematical analysis done in Chapter III. For clarity, the program contains comment statements which serve as a guide to the reader. The discussion in the following section is given so that the structure of the program will be understood.

A. Program Construction

In the computer program, the switching times are assigned new descriptive names and the text of this chapter, as well as those following, will conform to the assignment which is as follows:

Charging time (T_C): TCHARG

Dwell time (T_D): TDWELL

Energy dump time (T_E): TDUMP

Figure 4-1 shows a timing chart for the regulator and starting with a given set of initial conditions, the computer program must be able to simulate the cyclic process shown in this timing chart. Besides the load resistance R_L, some other component values are left as variables at the beginning of the program to allow changes to be made. These components are listed and identified at the beginning of the program.

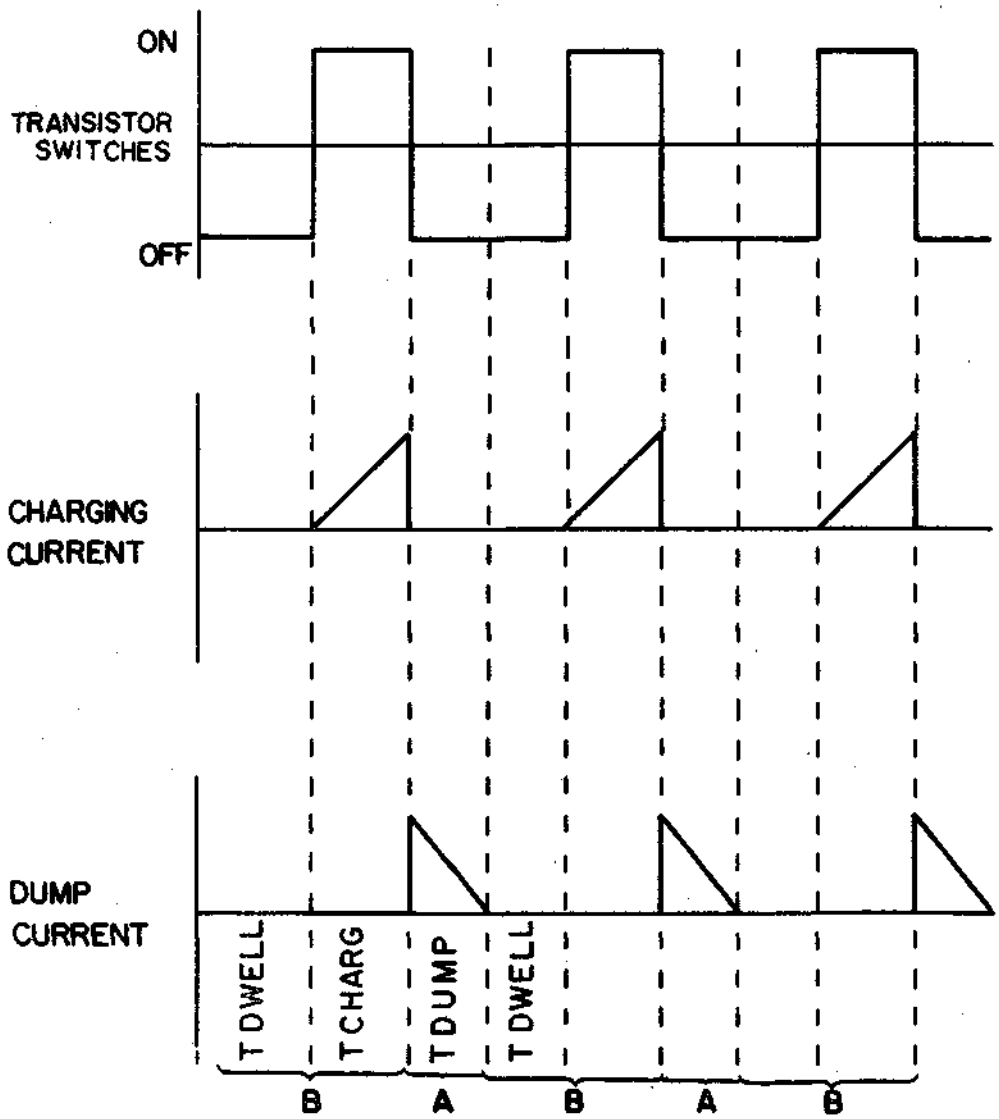

Figure 4-1. Timing chart showing sequence of the switching times.

For a given set of component values, the roots to the current equations (3-2 and 3-6) of the output filter are fixed. Since the roots are needed to determine the denominators and numerators of the partial-fraction-expansion forms of these current equations, they are calculated at the beginning. To do this, an IBM scientific subroutine called POLRT, for POLynomial RooTs, is used. All it requires are the coefficients of the denominators of Equations 3-2 and 3-6. Next in the program, the denominators of the partial fraction expansion are calculated and as indicated in Equation 3-3 and 3-7 they can be complex.

The above operations occupy blocks one through five in the program flowchart shown in Figure 4-2. It is intended that this chart show only the major functions to be performed and without details.

Blocks six through nineteen represent the cyclic action of the regulator. The process begins with the output filter in mode B; the transistor switches are off and the charging inductor contains no current. The length of time that the transistor switches remain off, TDWELL, must be calculated. Once TDWELL is known, CURNT(2) can be calculated at the end of that time and this current can be used to calculate TCHARG. During TCHARG the transistor switches will be on. As shown in the timing chart, at the end of TCHARG the switches will turn off and the charging inductors will begin to dump, placing the filter in mode A. Thus all filter currents and voltages must be calculated and used as new initial conditions for equations relating to mode A. Also CHARGI, the current through the charging inductor must be calculated. The filter will stay in mode A as long as the inductor is dumping. At the end of the dump time, TDUMP, the latest values of filter currents

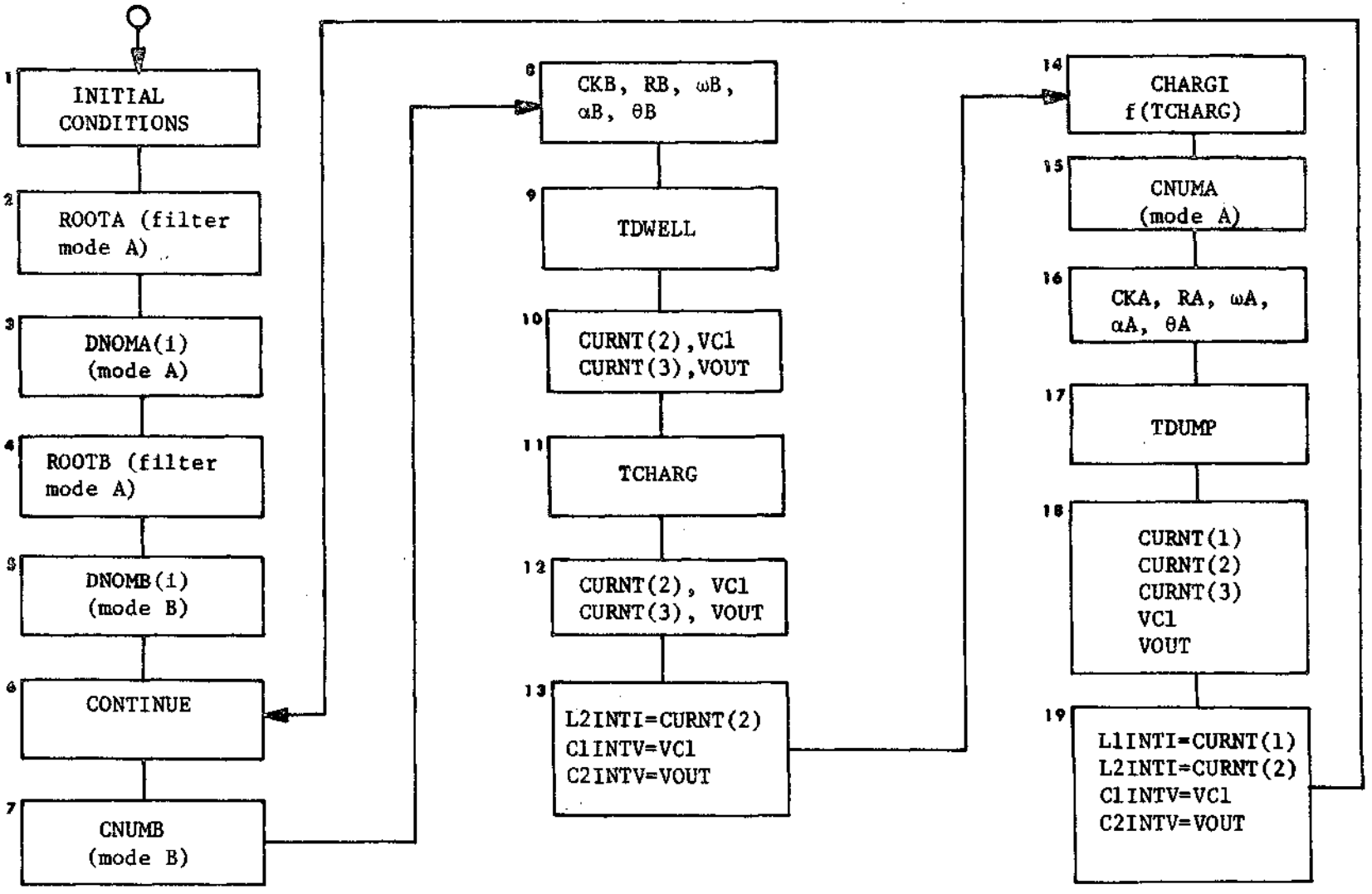

Figure 4-2. A simplified flowchart of the computer program.

and voltages are calculated and used as the initial conditions going into mode B. The cycle has been completed.

B. Program Listing

A listing of the computer program begins on page 56. First there is a glossary of terms to assist in following the program. This is followed by a list of components and initial conditions. Following the program listing, are the first two pages of a typical printout.

The computer source program is written in IBM System/360 FORTRAN IV which is compatible with USA FORTRAN. As stated previously, one IBM scientific subroutine, POLRT, is used. In addition, several built-in, FORTRAN-supplied mathematical function subprograms are used, such as Absolute value (ABS), Exponential (EXP), Natural logarithm (ALOG), and Sine (SIN).

The computer used was an IBM System/360 Model 50. To produce the plots given in Chapter VII, arrays to store data points were placed within the program and their contents plotted on a Calcomp Plotter.

```
C       ****  SWITCHING REGULATOR COMPUTER MODEL  ****
C
C
C
C       GLOSSARY OF TERMS USED IN THIS PROGRAM
C
C   ALPHAA, ALPHAB-  THE DAMPING FACTORS, EQUAL TO MINUS THE
C                    REAL PART OF THE OUTPUT FILTER'S ROOTS.
C   CHARGI-  CURRENT IN THE CHARGING INDUCTOR, L1.
C   CKA,CKB-  COEFFICIENTS OF PARTIAL FRACTION EXPANSION OF
C             CHARACTERISTIC EQUATIONS.
C   CNUMA, CNUMB-  NUMERATORS OF CHARACTERISTIC EQUATIONS,
C                  USED IN FINDING CKA AND CKB.
C   CURNT2-  MAGNITUDE OF THE CURRENT THROUGH L2.
C   C1INTV-  INITIAL VOLTAGE ON C1.
C   C2INTV-  INITIAL VOLTAGE ON C2.
C   C3INTV-  INITIAL VOLTAGE ON C3.
C   CYCLE-  RUNNING COUNT OF THE CYCLES THE REGULATOR HAS
C           GONE THROUGH.
C   DNOMA, DNOMB-  DENOMINATORS OF CHARACTERISTIC EQUATIONS,
C                  USED IN FINDING CKA AND CKB.
C   K1,K2-  CONSTANTS USED IN MODELING SATURATION
C           CHARACTERISTIC OF L1.
C   L1INTI-  INITIAL CURRENT THROUGH L1.
C   L2INTI-  INITIAL CURRENT THROUGH L2.
C   L1S-  ACTUAL INDUCTANCE VALUE OF L1, IT WILL BE A
C         FUNCTION OF THE CURRENT THROUGH IT.
C   N-  SUBSCRIPT FOR CALCULATED DATA POINTS, BEGINS AT 1.
C   MAXC-  MAXIMUM NUMBER OF CYCLES PROGRAMMER DESIRES THE
C          REGULATOR TO GO THROUGH.
C   OMEGAA, OMEGAB-  THE DAMPED NATURAL FREQUENCIES OF THE
C                    OUTPUT FILTER.  EQUAL TO THE POSITIVE
C                    IMAGINARY PART OF THE OUTPUT FILTER'S
C                    ROOTS.
C   RA, RB-  MAGNITUDE OF CURRENTS IN OUTPUT FILTER.
C   ROOTA, ROOTB-  ROOTS OF CHARACTERISTIC EQUATIONS OF
C                  OUTPUT FILTER.
C   T-  TIME.
C   TCHARG-  TIME FOR INPUT INDUCTOR, L1, TO CHARGE.
C   THETAA, THETAB-  PHASE ANGLE OF CURRENTS IN OUTPUT
C                    FILTER.
C   TTOTAL-  ACCUMULATED TIME, EQUALS SUM OF ALL TDWELLS,
C            TCHARGS, AND TDUMPS.
C   TDUMP-  TIME FOR INPUT INDUCTOR, L1, TO DUMP.
C   TDWELL-  REGULATOR DWELL TIME.  DURING THIS INTERVAL, THE
C            TRANSISTOR SWITCHES ARE OFF.
C   VC1-  VOLTAGE ACROSS THE INPUT CAPACITOR, C1, OF THE
C         OUTPUT FILTER.
```

```
C    VCURNT-  THE VOLTAGE AT THE NEGATIVE INPUT OF IC2-A16,
C             A COMPATATOR CIRCUIT WHICH DETERMINES TDWELL.
C    VIN-  REGULATOR INPUT VOLTAGE.
C    VOUT-  REGULATOR OUTPUT VOLTAGE.
C
      DIMENSION COF(4),XCOF(5),ROOTI(4),ROOTR(4),CURNT(3)
      DIMENSION RA(3,2),ALPHAA(2),THETAA(3,2),OMEGAA(2)
      DIMENSION RB(3,2),ALPHAB(2),THETAB(3,2),OMEGAB(2)
      COMPLEX ROOTA(4),CKA(3,4),CNUMA(3,4),DNOMA(4),S
      COMPLEX ROOTB(4),CKB(3,4),CNUMB(3,4),DNOMB(4)
      COMPLEX CMPLX
      REAL L1INTI,L2INTI,L1,L2,L1S,K1,K2,LC1,IDUMP
      INTEGER CYCLE
C
C
C    COMPONENT VALUES.
C
      C1 = 2640.0E-06
      C2 = 880.0E-06
      C3 = 180.E-6
      C6 = 1.1E-9
      L1 = 48.0E-06
      L2 = 480.0E-06
      LC1 = 0.003E-06
      R1 = 85.0E 03
      R2 = 4.99E 03
      R3 = 15.22E 03
      R12 = 750.0E 03
      R20 = 50.0E 03
      R21 = 400.0E 03
      R22 = 7.84E 03
      RD = 1.0E-03
      RL = 4.00
      RL1 = 10.0E-03
      RL2 = 60.0E-03
      RC1 = 10.0E-03
      RC2 = 10.0E-03
C
C    INITIAL VOLTAGES AND CURRENTS.
C
      VD = 0.6
      VIN = 60.00
      C1INTV = 29.50
      C2INTV = 29.50
      L1INTI = 0.0
C    THE FOLLOWING IS AN APPROXIMATION FOR L2INTI AND C3INTV.
      L2INTI = C2INTV/RL
      C3INTV = 0.90*R2/(R1+R2)*L2INTI
```

```
      VC1 = C1INTV
      VCURNT = C3INTV
      CURNT2 = ABS(L2INTI)
C
      CYCLE = 0
      MAXC = 500
      N = 1
      T = 0.0
      TTOTAL = 0.0
      K1 = 0.70E-06
      K2 = 1.08
C
      WRITE(6,380) VIN
      WRITE(6,390) RL
C
C    DETERMINE ROOTS OF FILTER.
C
      XCOF(1) = RL+RL2+RL1+RD
      XCOF(2) = L1+L2+C1*(RC1*RL2+(RL1+RD)*RC1+(RL1+RD)*RL2
     &          +RL*RC1+RL*(RL1+RD))+C2*(RL*RC2+RL*RL2+RC2*
     &          RL2+RL*(RL1+RD)+RC2*(RL1+RD))
      XCOF(3) = C2*L2*(RL+RC2)+C2*L1*(RL+RC2)+C1*L1*(RL+RC1
     &          +RL2)+C1*L2*(RC1+RL1+RD)+C1*C2*(RL*RC1*
     &          RC2+RL*RL2*RC1+RC1*RC2*RL2+RL*RC1*(RL1+RD)
     &          +RL*RC2*(RL1+RD)+RL*RL2*(RL1+RD)+RC1*RC2*
     &          (RL1+RD)+RC2*RL2*(RL1+RD))
      XCOF(4) = C1*L1*L2+C1*C2*L1*(RL*RC1+RL*RC2+RL*RL2+
     &          RC1*RC2+RC2*RL2)+C1*C2*L2*(RL*RC1+RL*(RL1+
     &          RD)+RC1*RC2+RC2*(RL1+RD))
      XCOF(5) = C1*C2*L1*L2*(RL+RC2)
      XCOFA1 = XCOF(1)
      XCOFA2 = XCOF(2)
      XCOFA3 = XCOF(3)
      XCOFA4 = XCOF(4)
      XCOFA5 = XCOF(5)
C
      WRITE(6,400)
      WRITE(6,410)
      WRITE(6,420)
C
      M = 4
      CALL POLRT(XCOF,COF,M,ROOTR,ROOTI,IER)
      DO 100 I=1,4
      ROOTA(I) = CMPLX(ROOTR(I),ROOTI(I))
      WRITE(6,430) I,ROOTR(I),ROOTI(I)
  100 CONTINUE
      DO 130 I=1,4
      S = ROOTA(I)
```

```
      DNOMA(I) = XCOF(5)
      K = 0
  110 K = K+1
      IF( K .EQ. I ) GO TO 110
      IF( K .GT. 4 ) GO TO 120
      DNOMA(I) = DNOMA(I)*(S-ROOTA(K))
      GO TO 110
  120 CONTINUE
  130 CONTINUE
      XCOF(1) = 1.0
      XCOF(2) = C2*RL+C2*RC2+C1*RL+C1*RC1+C1*RL2
      XCOF(3) = C1*L2+C1*C2*RC1*RL+C1*C2*RC1*RC2+C1*C2*RL2*
     &          RL+C1*C2*RL2*RC2+C1*C2*RC2*RL
      XCOF(4) = C1*C2*L2*RL+C1*C2*L2*RC2
      XCOF(5) = 0.0
C
      WRITE(6,400)
      WRITE(6,440)
      WRITE(6,420)
C
      M = 3
      CALL POLRT(XCOF,COF,M,ROOTR,ROOTI,IER)
      DO 140 I=1,3
      ROOTB(I) = CMPLX(ROOTR(I),ROOTI(I))
      WRITE(6,430) I,ROOTR(I),ROOTI(I)
  140 CONTINUE
      DO 170 I=1,3
      S = ROOTB(I)
      DNOMB(I) = XCOF(4)
      K = 0
  150 K = K+1
      IF( K .EQ. I ) GO TO 150
      IF( K .GT. 3 ) GO TO 160
      DNOMB(I) = DNOMB(I)*(S-ROOTB(K))
      GO TO 150
  160 CONTINUE
  170 CONTINUE
C
      WRITE(6,450)
      WRITE(6,460) C1INTV,L1INTI
      WRITE(6,470) C2INTV,L2INTI
      WRITE(6,480) C3INTV
C
  180 CONTINUE
C   WITH STATEMENT 180, THE REGULATOR CYCLE BEGINS.
C
C   CYCLE EQUALS THE CYCLE NUMBER THE REGULATOR IS ABOUT
C   TO GO THROUGH.
```

```
C
      CYCLE = CYCLE+1
      WRITE(6,490) CYCLE,TTOTAL
C
      DO 190 I=1,3
      S = ROOTB(I)
  190 CNUMB(2,I) = S**2*(C1*C2*(RL+RC2)*L2*L2INTI)+S*(C1*
     &              L2*L2INTI+C1*C2*((RL+RC2)*C1INTV-RL*
     &              C2INTV))+C1*C1INTV
      DO 200 I = 1,3
      S = ROOTB(I)
  200 CNUMB(3,I) = S**2*(C1*C2*(L2*C2INTV+RC2*L2*L2INTI))+S*
     &              (C1*C2*((RC1+RL2)*C2INTV+RC2*C1INTV)+C1
     &              *L2*L2INTI)+(C1*C1INTV+C2*C2INTV)
C
C   NOW CALCULATE THE COEFICIENTS, FREQUENCIES AND
C   DAMPING FACTORS OF THE LOOP CURRENTS WHILE THE
C   FILTER IS IN MODE B.
C
      DO 240 I = 2,3
      DO 230 J = 1,3
      IF( AIMAG(ROOTB(J)) ) 230,220,210
  210 CKB(I,1) = CNUMB(I,J)/DNOMB(J)
      RB(I,1) = CABS(CKB(I,1))
      TOPB = AIMAG(CKB(I,1))
      BOTB = REAL(CKB(I,1))
      THETAB(I,1) = ATAN2(TOPB,BOTB)
      OMEGAB(1) = AIMAG(ROOTB(J))
      ALPHAB(1) = -REAL(ROOTB(J))
      GO TO 230
  220 CKB(I,2) = CNUMB(I,J)/DNOMB(J)
      RB(I,2) = CKB(I,2)
      ALPHAB(2) = -ROOTB(J)
  230 CONTINUE
  240 CONTINUE
C
C   NOW CALCULATE TDWELL.
C
      TDWELL = ((VCURNT*(7.5E3+R3)-15.0*R3)/7.5E3+VC1)
     &          *C1/CURNT2
      IF( TDWELL .LT. 0.0 ) TDWELL=0.0
      T = TDWELL
C
C   NOW CALCULATE THE FILTER CURRENTS AND VOLTAGES
C   DURING TDWELL.
C
      HH = THETAB(2,1)-ATAN2(OMEGAB(1),-ALPHAB(1))
      SQB = SQRT(ALPHAB(1)**2+OMEGAB(1)**2)
```

```
      DT1 = T/5.0
      CURNT(1) = 0.0
      DO 250 K= 1,5
      T = FLOAT(K)*DT1
C
      CHARGI = 0.0
      CURNT(2) = 2.*RB(2,1)*EXP(-ALPHAB(1)*T)*COS(OMEGAB(1)
     &           *T+THETAB(2,1))+RB(2,2)*EXP(-ALPHAB(2)*T)
      CURNT(3) = 2.*RB(3,1)*EXP(-ALPHAB(1)*T)*COS(OMEGAB(1)
     &           *T+THETAB(3,1))+RB(3,2)*EXP(-ALPHAB(2)*T)
      VC1 = -1/C1*(2*RB(2,1)*EXP(-ALPHAB(1)*T)/SQB*
     &      COS(OMEGAB(1)*T+HH)+RB(2,2)/(-ALPHAB(2))*
     &      EXP(-ALPHAB(2)*T))+1.0/C1*(2.0*RB(2,1)/
     &      SQB*COS(HH)+RB(2,2)/(-ALPHAB(2)))+C1INTV-
     &      RC1*CURNT(2)
      VOUT = RL*CURNT(3)
      TTOTAL = TTOTAL+DT1
      N = N+1
  250 CONTINUE
C
      WRITE(6,500) TDWELL
      WRITE(6,510) CURNT(1),CHARGI
      WRITE(6,520) CURNT(2),VC1
      WRITE(6,530) CURNT(3),VOUT
C
C
C   NOW CALCULATE TCHARG.
C
      V1 = 0.20*CURNT2
      THING = ((R12+R20)/(R21+R22)*(V1+0.6)+VIN+0.6)/(VIN-V1)
      TCHARG = (R12+R20)*(R21+R22)*C6/(R12+R20+R21+R22)
     &         *ALOG(THING)
C
C   NOW CALCULATE THE FILTER CURRENTS AND VOLTAGES
C   DURING TCHARG.
C
      CHARGI = 0.0
      T = TCHARG
      TOLD = 0.0
      T1 = 0.0
      K = 1
      DT2 = T/50.0
      DO 260 I=1,50
      L1S = 4.0*(L1-K1*CHARGI**K2)
      DELI = VIN*DT2/L1S
      CHARGI = CHARGI+DELI
      T1 = T1+DT2
      IF( I .EQ. 1 ) GO TO 255
```

```
      IF( I .NE. 10*K ) GO TO 260
      K = K+1
  255 CONTINUE
      T = TOWELL+T1
      CURNT(2) = 2.*RB(2,1)*EXP(-ALPHAB(1)*T)*COS(OMEGAB(1)
     &           *T+THETAB(2,1))+RB(2,2)*EXP(-ALPHAB(2)*T)
      CURNT(3) = 2.*RB(3,1)*EXP(-ALPHAB(1)*T)*COS(OMEGAB(1)
     &           *T+THETAB(3,1))+RB(3,2)*EXP(-ALPHAB(2)*T)
      VC1 = -1/C1*(2*RB(2,1)*EXP(-ALPHAB(1)*T)/SQB*
     &      COS(OMEGAB(1)*T+HH)+RB(2,2)/(-ALPHAB(2))*
     &      EXP(-ALPHAB(2)*T))+1.0/C1*(2.0*RB(2,1)/
     &      SQB*COS(HH)+RB(2,2)/(-ALPHAB(2)))+C1INTV-
     &      RC1*CURNT(2)
      VOUT = RL*CURNT(3)
      TTOTAL = TTOTAL+T1-TOLD
      TOLD = T1
      N = N+1
  260 CONTINUE
      CURNT2 = ABS(CURNT(2))
      VCURNT = 0.90*CURNT2*R2/(R1+R2)-(0.90*CURNT2*R2/(R1
     &         +R2)-C3INTV)*EXP(-(R1+R2)/(R1*R2*C3)*T)
C
      WRITE(6,540) TCHARG
      WRITE(6,510) CURNT(1),CHARGI
      WRITE(6,520) CURNT(2),VC1
      WRITE(6,530) CURNT(3),VOUT
C
C   UPDATE INITIAL CONDITIONS.
C
      L1INTI = 4.0*CHARGI
      L2INTI = CURNT(2)
      C1INTV = VC1+RC1*CURNT(2)
      C2INTV = VOUT
      C3INTV = VCURNT
      CURNT1 = CHARGI
      CHARGI = 0.0
C
C   NOW THE INPUT INDUCTOR HAS BEEN CHARGED AND IS GOING TO
C   DUMP AND THE FILTER WILL BE IN MODE A.
C
      DO 270 I=1,4
      S = ROOTA(I)
  270 CNUMA(1,I) = S**3*(C1*C2*L2*(RL+RC2)*L1*L1INTI)+S**2*(
     &             C1*L2*L1*L1INTI+C1*C2*(RL*RC1+RL*RC2+RL*
     &             RL2+RC1*RC2+RC2*RL2)*L1*L1INTI-C1*C2*L2*
     &             (RL+RC2)*C1INTV-C1*C2*L2*(RL+RC2)*VD+C1*
     &             C2*(RL*RC1+RC1*RC2)*L2*L2INTI)+S*(C2*(RL
     &             +RC2)*L1*L1INTI+C1*RL*L1*L1INTI+C1*(RC1+
```

```
     &              RL2)*L1*L1INTI-C1*L2*C1INTV-C1*C2*(RL*RC2
     &              +RL*RL2+RC2*RL2)*C1INTV-C1*L2*VD-C1*C2*(
     &              RL*RC1+RL*RC2+RL*RL2+RC1*RC2+RC2*RL2)*VD
     &              +C2*(RL+RC2)*L2*L2INTI+C1*RC1*L2*L2INTI-
     &              C1*C2*RC1*RL*C2INTV)+(L1*L1INTI+L2*
     &              L2INTI-C1*(RL+RL2)*C1INTV+C2*(RL+RC2)*VD
     &              -C1*(RL+RC1+RL2)*VD-C2*RL*C2INTV)
     &              -(-VD/(RL+RL2+RL1+RD))*(S**3*
     &              XCOFA5+S**2*XCOFA4+S*XCOFA3+XCOFA2)
      DO 280 I=1,4
      S = ROOTA(I)
  280 CNUMA(2,I) = S**3*(C1*C2*L1*(RL+RC2)*L2*L2INTI)+S**2*
     &              (C1*L1*L2*L2INTI+C1*C2*L1*(RL+RC2)*C1INTV
     &              -C1*C2*L1*RL*C2INTV+C1*C2*(RL*RC1+RL*(RL1
     &              +RD)+RC1*RC2+RC2*(RL1+RD))*L2*L2INTI+C1*
     &              C2*RC1*(RL+RC2)*L1*L1INTI)+S*(C2*(RL+RC2
     &              )*L2*L2INTI+C1*(RC1+RL1+RD)*L2*L2INTI+C1
     &              *C2*(RL*(RL1+RD)+RC2*(RL1+RD))*C1INTV-C1
     &              *C2*(RL*RC1+RL*(RL1+RD))*C2INTV+C2*(RL+RC2
     &              )*L1*L1INTI+C1*RC1*L1*L1INTI-C1*C2*RC1*(
     &              RL+RC2)*VD+C1*L1*C1INTV)+(L1*L1INTI+L2*
     &              L2INTI-C2*RL*C2INTV+C1*(RL1+RD)*C1INTV-C2
     &              *(RL+RC2)*VD-C1*RC1*VD)
     &              -(-VD/(RL1+RD+RL2+RL))*(S**3*
     &              XCOFA5+S**2*XCOFA4+S*XCOFA3+XCOFA2)
      DO 290 I=1,4
      S = ROOTA(I)
  290 CNUMA(3,I) = S**3*(C1*C2*L1*L2*C2INTV+C1*C2*L1*RC2*L2
     &              *L2INTI)+S**2*(C1*C2*L1*(RC1+RL2)*C2INTV
     &              +C1*L1*L2*L2INTI+C1*C2*L1*RC2*C1INTV+C1*C2*
     &              L2*(RC1+RL1+RD)*C2INTV+C1*C2*(RC1+RL1+RD)
     &              *RC2*L2*L2INTI+C1*C2*RC1*RC2*L1*L1INTI)+
     &              S*(C2*L2*C2INTV+C2*RC2*L2*L2INTI+C2*L1*
     &              C2INTV+C1*L1*C1INTV+C1*C2*(RC1*RL2+RC1*(RL1
     &              +RD)+RL2*(RL1+RD))*C2INTV+C1*(RC1+RL1+RD)*
     &              L2*L2INTI+C1*C2*RC2*(RL1+RD)*C1INTV+C2*RC2*
     &              L1*L1INTI+C1*RC1*L1*L1INTI-C1*C2*RC1*RC2*
     &              VD)+(L1*L1INTI+L2*L2INTI+C2*RL2*C2INTV+C2
     &              *(RL1+RD)*C2INTV+C1*(RL1+RD)*C1INTV-C2*
     &              RC2*VD-C1*RC1*VD)
     &              -(-VD/(RL1+RD+RL2+RL))*(S**3*XCOFA5+S**2*
     &              XCOFA4+S*XCOFA3+XCOFA2)
C
C    NOW CALCULATE COEFICIENTS, FREQUENCIES AND DAMPING FACTOR
C    OF THE LOOP CURRENTS WHILE THE FILTER IS IN MODE A.
C
      DO 340 I=1,3
      K = 1
```

```
      DO 330 J=1,4
      IF( AIMAG(ROOTA(J)) ) 330,330,300
  300 GO TO (310,320),K
  310 CKA(I,1) = CNUMA(I,J)/DNOMA(J)
      RA(I,1) = CABS(CKA(I,1))
      TOPA = AIMAG(CKA(I,1))
      BOTA = REAL(CKA(I,1))
      THETAA(I,1) = ATAN2(TOPA,BOTA)
      K = 2
      IF(I .GT. 1) GO TO 330
      OMEGAA(1) = AIMAG(ROOTA(J))
      ALPHAA(1) = -REAL(ROOTA(J))
      GO TO 330
  320 CKA(I,2) = CNUMA(I,J)/DNOMA(J)
      RA(I,2) = CABS(CKA(I,2))
      TOPA = AIMAG(CKA(I,2))
      BOTA = REAL(CKA(I,2))
      THETAA(I,2) = ATAN2(TOPA,BOTA)
      IF(I .GT. 1) GO TO 330
      OMEGAA(2) = AIMAG(ROOTA(J))
      ALPHAA(2) = -REAL(ROOTA(J))
  330 CONTINUE
  340 CONTINUE
C
C   NOW CALCULATE TDUMP.
C
      K = 1
      T2 = 0.0
      DT3 = 0.0
      TOLD = 0.0
      DELI = CURNT1/40.0
      DO 360 I=1,41
      L1S = 4.0*(L1-K1*(DELI*(41-I))**K2)
      T2 = T2+DT3
      DT3 = DELI*L1S/(VC1+0.6)
      IF( I-1 .LE. 2 ) GO TO 350
      IF( (I-1) .NE. K*5 ) GO TO 360
      K = K+1
  350 T = T2
      TDUMP = T
C
C   NOW CALCULATE FILTER CURRENTS AND VOLTAGES WHEN THE INPUT
C   INDUCTOR BEGINS TO DUMP.
C
      CURNT(1) = 4.0*(DELI*(41-I))
      IDUMP = CURNT(1)
      CURNT(2) = 2.*RA(2,1)*EXP(-ALPHAA(1)*T)*COS(OMEGAA(1)*T+
     &           THETAA(2,1))+2.*RA(2,2)*EXP(-ALPHAA(2)*T)*COS
```

```
     &            (OMEGAA(2)*T+THETAA(2,2))-VD/(RL1+RD+RL2+RL)
      CURNT(3) = 2.*RA(3,1)*EXP(-ALPHAA(1)*T)*COS(OMEGAA(1)*T+
     &           THETAA(3,1))+2.*RA(3,2)*EXP(-ALPHAA(2)*T)*COS
     &           (OMEGAA(2)*T+THETAA(3,2))-VD/(RL1+RD+RL2+RL)
       VLC1 = -LC1*4.0*DELI/DT3
       IF( T .LT. 2.0E-06 ) VLC1=LC1*L1INTI/1.0E-06
       VC1 = 1.0/C1*(-4.0*DELI/(2.0*DT3)*T**2+(L1INTI-
     &      CURNT(2))*T)+C1INTV+RC1*(CURNT(1)-CURNT(2))+VLC1
       VOUT = RL*CURNT(3)
       TTOTAL = TTOTAL+T-TOLD
       TOLD = T
       N = N+1
  360 CONTINUE
C
       CURNT2 = ABS(CURNT(2))
       VCURNT = 0.90*CURNT2*R2/(R1+R2)-(0.90*CURNT2*R2/(R1
     &          +R2)-C3INTV)*EXP(-(R1+R2)/(R1*R2*C3)*T)
C
       WRITE(6,550) TDUMP
       WRITE(6,510) CURNT(1),CHARGI
       WRITE(6,520) CURNT(2),VC1
       WRITE(6,530) CURNT(3),VOUT
C
C    UPDATE INITIAL CONDITIONS.
C
       L1INTI = CURNT(1)
       L2INTI = CURNT(2)
       C1INTV = VC1+RC1*CURNT(2)
       C2INTV = VOUT
       C3INTV = VCURNT
C
C
C    THE CHARGING INDUCTOR HAS DUMPED AND THE LATEST FILTER
C    CURRENTS AND VOLTAGES HAVE BEEN CALCULATED.  NOW RETURN
C    TO STATEMENT 180 AND START ANOTHER CYCLE OR END.
C
       IF( CYCLE .GE. MAXC ) GO TO 370
       GO TO 180
  370 CONTINUE
C
  380 FORMAT('2',25X,'INPUT VOLTAGE = VIN = ',F11.4)
  390 FORMAT('0',25X,'LOAD RESISTANCE = RL = ',F10.4)
  400 FORMAT('-',///,17X,'THE FOLLOWING ARE THE ROOTS TO',
     &       ' THE OUTPUT FILTER')
  410 FORMAT(' ',16X,'WHILE IT IS IN MODE A.')
  420 FORMAT('-',34X,'REAL PART',7X,'IMAG PART')
  430 FORMAT('0',23X,'ROOT(',I1,') = ',E12.5,4X,E12.5)
  440 FORMAT(' ',16X,'WHILE IT IS IN MODE B.')
```

```
  450 FORMAT('1',18X,'STARTING INITIAL CONDITIONS')
  460 FORMAT('-',21X,'C1INTV = ',E11.4,4X,'L1INTI = ',E11.4)
  470 FORMAT(' ',21X,'C2INTV = ',E11.4,4X,'L2INTI = ',E11.4)
  480 FORMAT(' ',21X,'C3INTV = ',E11.4,///)
  490 FORMAT('0',15X,'BEGINNING CYCLE NUMBER ',I4,5X,
     &       'TTOTAL = ',E11.4)
  500 FORMAT('0',21X,'VALUES AT THE END OF TDWELL = ',E11.4)
  510 FORMAT(' ',25X,'CURNT(1) = ',E11.4,2X,'CHARGI = ',E11.4)
  520 FORMAT(' ',25X,'CURNT(2) = ',E11.4,5X,'VC1 = ',E11.4)
  530 FORMAT(' ',25X,'CURNT(3) = ',E11.4,4X,'VOUT = ',E11.4)
  540 FORMAT('0',21X,'VALUES AT THE END OF TCHARG = ',E11.4)
  550 FORMAT('0',21X,'VALUES AT THE END OF TDUMP = ',E11.4)
C
      STOP
      END
```

INPUT VOLTAGE = VIN = 60.0000

LOAD RESISTANCE = RL = 4.0000

THE FOLLOWING ARE THE ROOTS TO THE OUTPUT FILTER WHILE IT IS IN MODE A.

	REAL PART	IMAG PART
ROOT(1) =	-0.21639E 03	-0.14385E 04
ROOT(2) =	-0.21639E 03	0.14385E 04
ROOT(3) =	-0.22736E 03	-0.29852E 04
ROOT(4) =	-0.22736E 03	0.29852E 04

THE FOLLOWING ARE THE ROOTS TO THE OUTPUT FILTER WHILE IT IS IN MODE B.

	REAL PART	IMAG PART
ROOT(1) =	-0.70653E 02	0.0
ROOT(2) =	-0.18967E 03	-0.17690E 04
ROOT(3) =	-0.18967E 03	0.17690E 04

```
   STARTING INITIAL CONDITIONS

      C1INTV =  0.2950E 02     L1INTI =  0.0
      C2INTV =  0.2950E 02     L2INTI =  0.7375E 01
      C3INTV =  0.3681E 00


BEGINNING CYCLE NUMBER    1      TTOTAL =  0.0

      VALUES AT THE END OF TDWELL =  0.6263E-04
          CURNT(1) =  0.0          CHARGI =  0.0
          CURNT(2) =  0.7297E 01     VC1 =  0.2925E 02
          CURNT(3) =  0.7374E 01    VOUT =  0.2950E 02

      VALUES AT THE END OF TCHARG =  0.2967E-04
          CURNT(1) =  0.0          CHARGI =  0.1008E 02
          CURNT(2) =  0.7252E 01     VC1 =  0.2917E 02
          CURNT(3) =  0.7373E 01    VOUT =  0.2949E 02

      VALUES AT THE END OF TDUMP =  0.5872E-04
          CURNT(1) =  0.0          CHARGI =  0.0
          CURNT(2) =  0.7215E 01     VC1 =  0.2950E 02
          CURNT(3) =  0.7371E 01    VOUT =  0.2948E 02

BEGINNING CYCLE NUMBER    2      TTOTAL =  0.1510E-03

      VALUES AT THE END OF TDWELL =  0.6337E-04
          CURNT(1) =  0.0          CHARGI =  0.0
          CURNT(2) =  0.7150E 01     VC1 =  0.2933E 02
          CURNT(3) =  0.7367E 01    VOUT =  0.2947E 02

      VALUES AT THE END OF TCHARG =  0.2922E-04
          CURNT(1) =  0.0          CHARGI =  0.9912E 01
          CURNT(2) =  0.7113E 01     VC1 =  0.2925E 02
          CURNT(3) =  0.7365E 01    VOUT =  0.2946E 02

      VALUES AT THE END OF TDUMP =  0.5771E-04
          CURNT(1) =  0.0          CHARGI =  0.0
          CURNT(2) =  0.7090E 01     VC1 =  0.2956E 02
          CURNT(3) =  0.7360E 01    VOUT =  0.2944E 02

BEGINNING CYCLE NUMBER    3      TTOTAL =  0.3013E-03
```

V. THE AC OUTPUT IMPEDANCE

It is possible to calculate the ac output impedance of a regulator as a function of frequency and use the result to obtain an insight into the regulation of the system. The regulator's output stage is a low-pass filter usually composed of one or more π-filter sections each of which is composed of inductors and capacitors having some series equivalent resistance. The output impedance will exhibit resonances, or zeros and poles of impedances, at certain frequencies. At the poles, the impedance of the filter becomes relatively large and may reach a value that will lead to poor voltage regulation. Thus, a design requirement is to choose component values that will place the resonance points outside the range of any frequencies that might be introduced by fluctuating loads.

One common method of calculating the ac output impedance is to inactivate all independent sources and mathematically apply a test voltage, $v_T(f,t)$, at the output. The scripts (f,t) indicate that the voltage $v_T(f,t)$ will be a function of frequency and time. The ac output impedance is equal to the ratio of the phasor equivalents of the voltage applied at the output and the resulting current. When linear feedback signals are present in the regulator, they must be accounted for by realizing that they are dependent sources and must be included in calculating the output impedance which can be done by using linear analysis techniques.

When nonlinearities are present, analysis becomes more complicated and often leads to tedious calculations which force one to seek appropriate simplifications. Consider now the CBRM regulator which has two sources of nonlinearity as shown in Figure 5-1, a simplified model of the regulator. The nonlinearities are due to the switching modulator and the circuitry that generates a feedback voltage, FB_2, proportional to the absolute magnitude of the current in the second loop of the output filter. In this system then, an unrestricted linear analysis cannot be used due to the presence of frequencies, other than the original, produced by these nonlinear devices. Rather than perform a nonlinear analysis on the CBRM regulator, a piecewise-linear analysis will be done. To justify this, it will be shown that the influence of the nonlinear feedback signal, FB_2, becomes negligible when the frequency of $v_T(f,t)$ exceeds a low-frequency range, and it will also be shown that the switching modulator can be linearly modeled. In this manner, a restricted model will be produced for which the ac output impedance will be developed. Before covering the nonlinear feedback path, the switching modulator will be discussed.

Since the switching frequency is much higher than the cutoff frequency of the output filter, it is assumed that the ripple components reaching the feedback connections are small and any ripple components reaching the input to the modulator can be neglected. With this assumption, the output voltage of the switching modulator can be replaced by its average value as far as its effect on the output and feedback voltage is concerned. As discussed in Chapter II, the average value of the switching modulator output voltage is a function of its duty cycle which

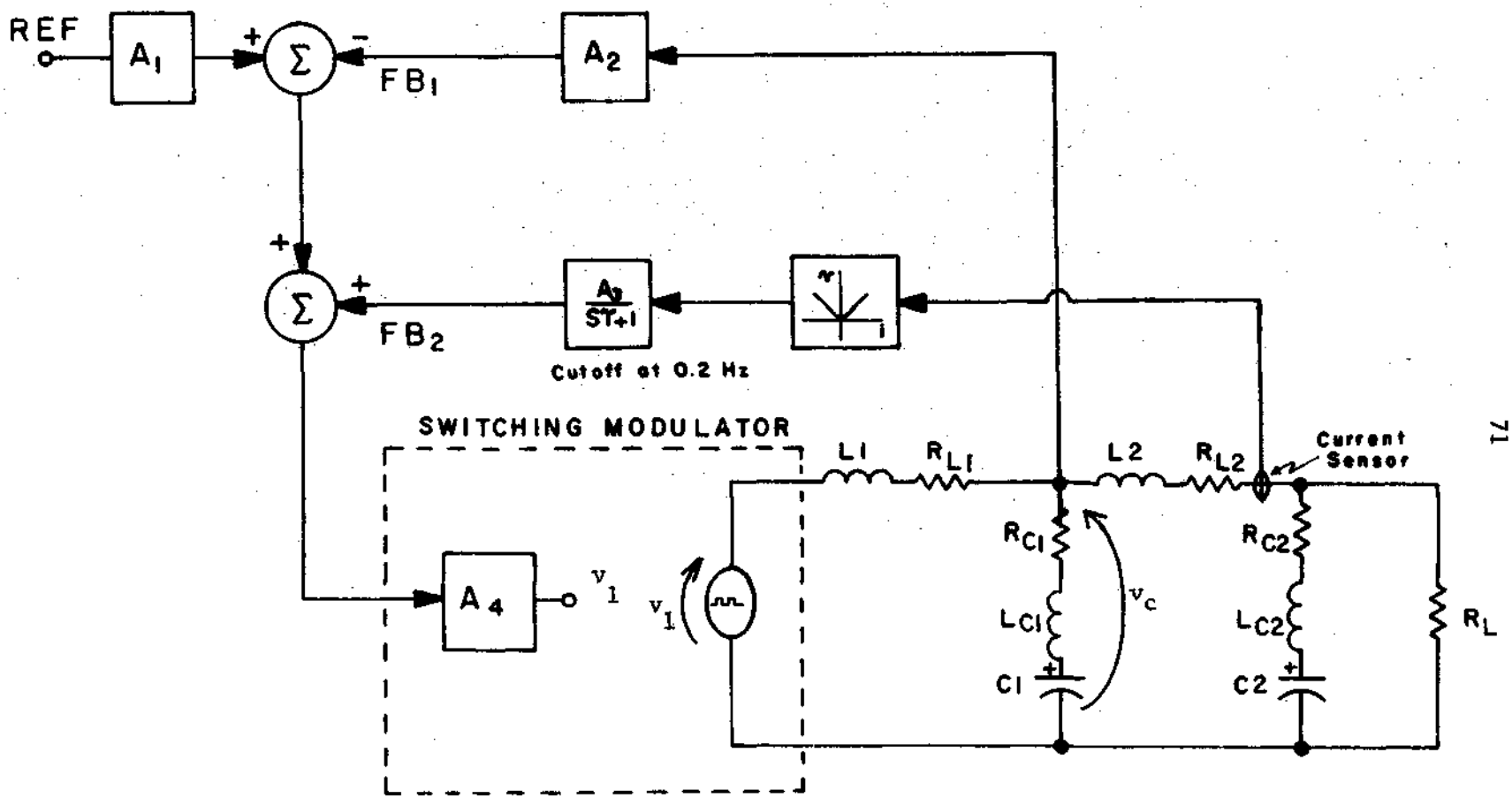

Figure 5-1. A simplified nonlinear model of the regulator.

in turn is a function of the modulator's input voltage. Based on the above discussion, the switching modulator can be modeled as a voltage-controlled voltage source to obtain the linear model shown in Figure 5-2. The Justification for eliminating the nonlinear feedback path will now be given.

Considering the nonlinear feedback path in Figure 5-1, the feedback signal, FB_2, is a voltage resulting from monitoring the magnitude of the current in the second loop of the filter. The path gain, A_3, has a value of approximately 0.55 and a cutoff frequency of approximately 0.2 Hz. The feedback signal FB_1 is a voltage proportional to the voltage v_c and is summed with a fraction of the reference voltage. The gains A_1 and A_2 are produced by a voltage divider network and have values of approximately 0.67 and 0.33, respectively.

For frequencies greater than ten times the cutoff frequency, 0.2 Hz, the feedback signal FB_2 becomes small and its influence on the system is negligible when compared with FB_1. Since v_c will be large at low frequencies, FB_1 will be large. At higher frequencies, FB_1 will decrease but so will FB_2. Thus, FB_1 will have the dominant influence once the cutoff frequency of the FB_2 path is exceeded. However, note that there is a high frequency range reached for which all feedback will be negligible and the output impedance will be determined by the resistance and inductance of the capacitor in the filter's output branch. This is true since the capacitors offer little impedance and the inductance of L2, a filter inductor, is many times greater than L_{C2} which is the small series equivalent inductance of C2. If the frequency of $v_T(f,t)$ is restricted to values greater than the 0.2 Hz cutoff value,

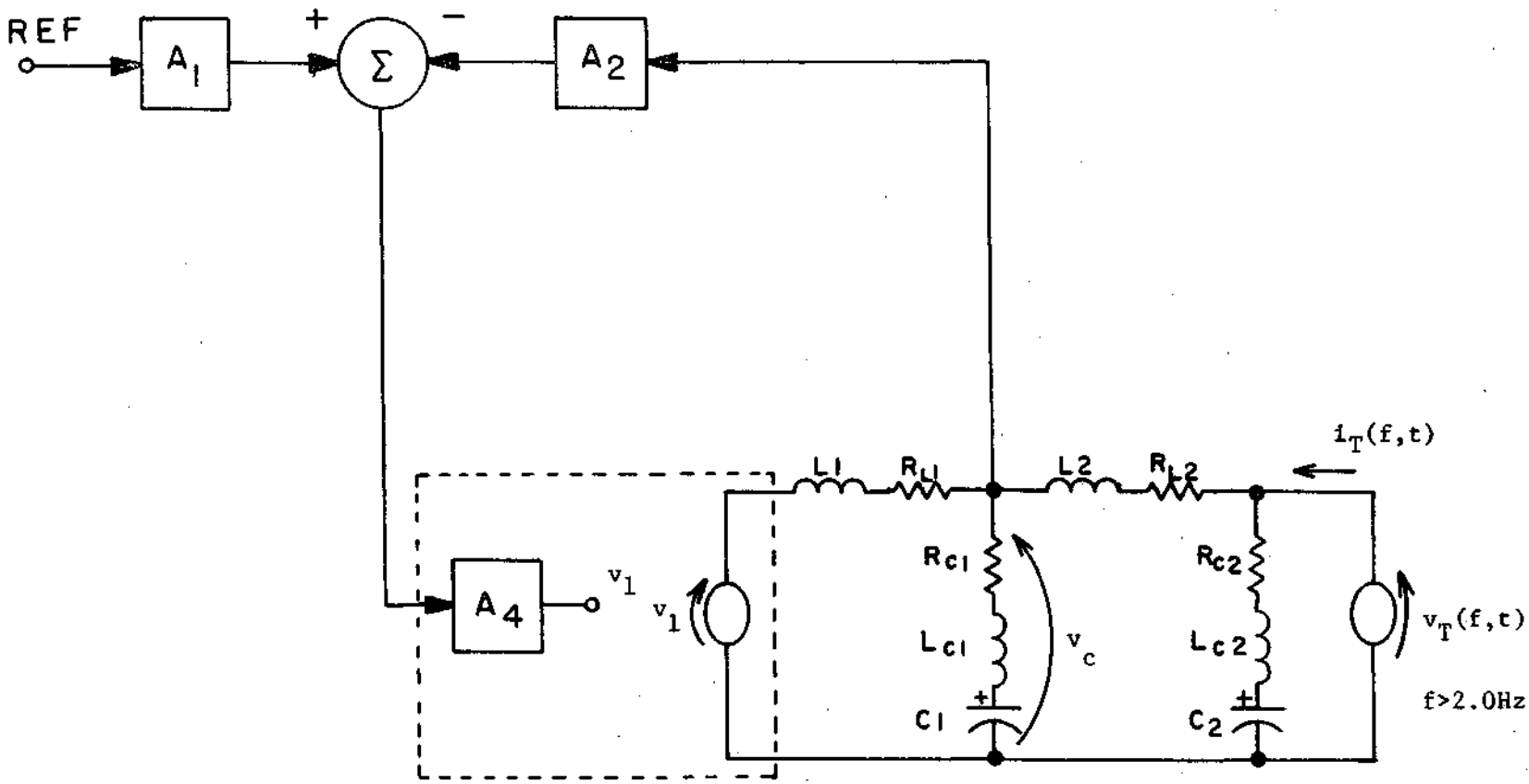

Figure 5-2. A restricted simplified linear model of the regulator.

the nonlinear feedback path can be neglected leaving the linear system shown in Figure 5-2.

Before the ac output impedance can be calculated for the restricted linear model, the value of A_4 must be determined. To do this, it is recalled from Chapter II that the purpose of the current monitor and associated circuitry was to force a reduction in output voltage as a function of output current. The resulting characteristic is shown in Figure 5-3. This response, good for slow changes in load current, yields an effective dc resistance of 213 milliohms. Using this value and solving ratio $v_T(0,t)/i_T(0,t)$ produces a value of approximately 100 for A_4.

Now solving for the ac output impedance, $Z(\omega)$, of the circuit in Figure 5-2 yields:

$$Z(\omega) = \frac{B_1B_4(B_2 + B_3) + B_2B_3B_4(1 + K)}{B_1(B_2 + B_3 + B_4) + B_2(B_3 + B_4)(1 + K)} \qquad (5\text{-}1)$$

where $K = A_2A_4$

$B_1 = R_{L1} + j\omega L1$

$B_2 = R_{C1} + j(\omega L_{C1} - 1/\omega C1)$

$B_3 = R_{L2} + j\omega L2$

and $B_4 = R_{C2} + j(\omega L_{C2} - 1/\omega C2)$.

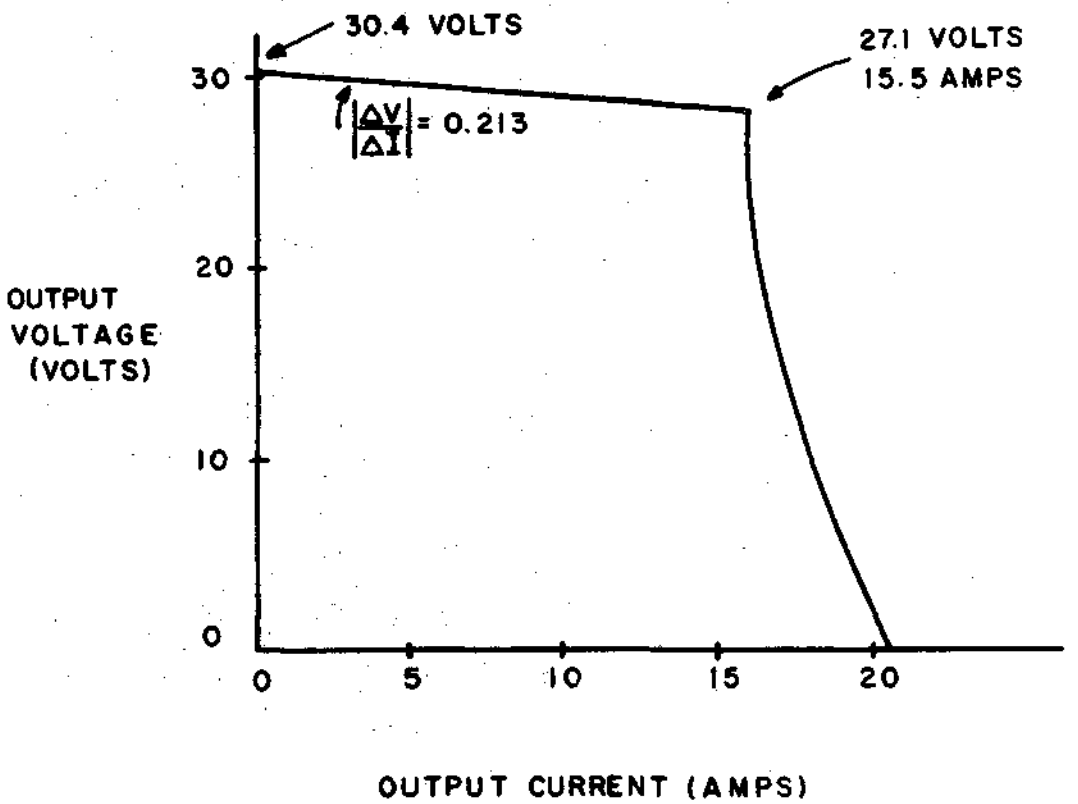

Figure 5-3. The output voltage/output current characteristic showing the programmed slope.

The magnitude of the ac impedance was calculated and plotted for a range of frequencies and is shown in Figure 5-4. Also shown on the same plot is the magnitude of the impedance due just to the output filter, i.e., with no feedback.

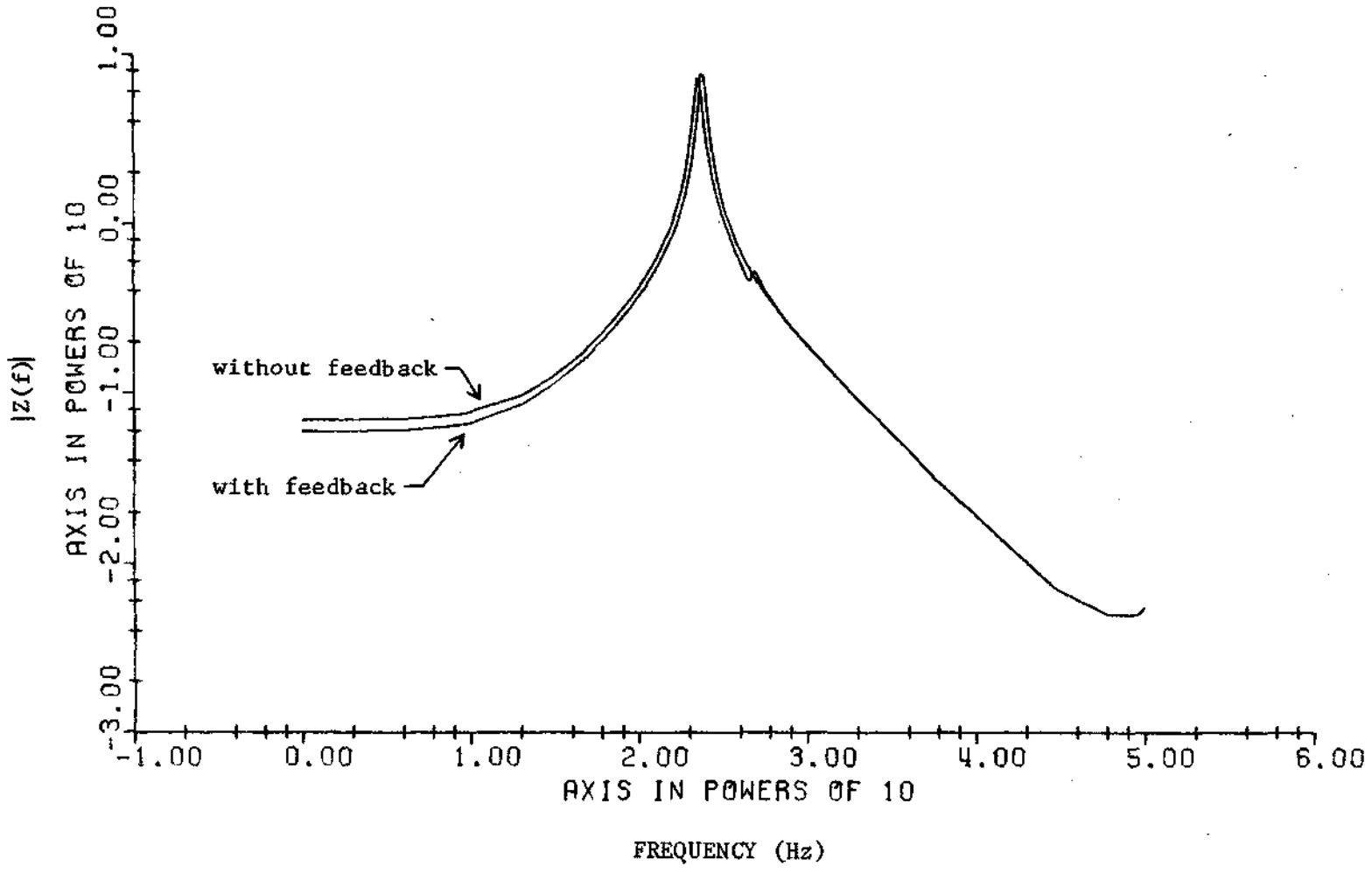

Figure 5-4. Magnitude of ac output impedance as a function of frequency.

VI. POWER SHARING

Now that the single regulator has been modeled and analyzed, a study will be made of the complete power system in which eighteen such regulators are paralleled and are under the control of a power sharing feedback network.

It was found in the previous analysis that the Thevenin voltage of the regulator was approximately 30.4 volts and the Thevenin resistance was approximately 213 milliohms. Thus, the general expression for the output voltage, in this chapter called V_1, as a function of the load current, I_m, is:

$$V_1 = V_{R2} - R_s I_m \tag{6-1}$$

where V_{R2} and R_s is the Thevenin voltage and Thevenin resistance, respectively. The value of V_1 is in the range of 27 to 30 volts, depending on the current demand which could be as large as 15.5 amperes.

Figure 6-1 illustrates how one regulator is connected to the output power bus and is under the influence of the power sharing circuit. With no feedback, i.e., V_f equal to zero, the regulator portion of the figure is a model for Equation 6-1. The feedback voltage, V_f, is developed as follows. The output bus voltage, V_B, is compared with a reference voltage, V_{R1}, of 29.5 volts and the difference is amplified by A_1

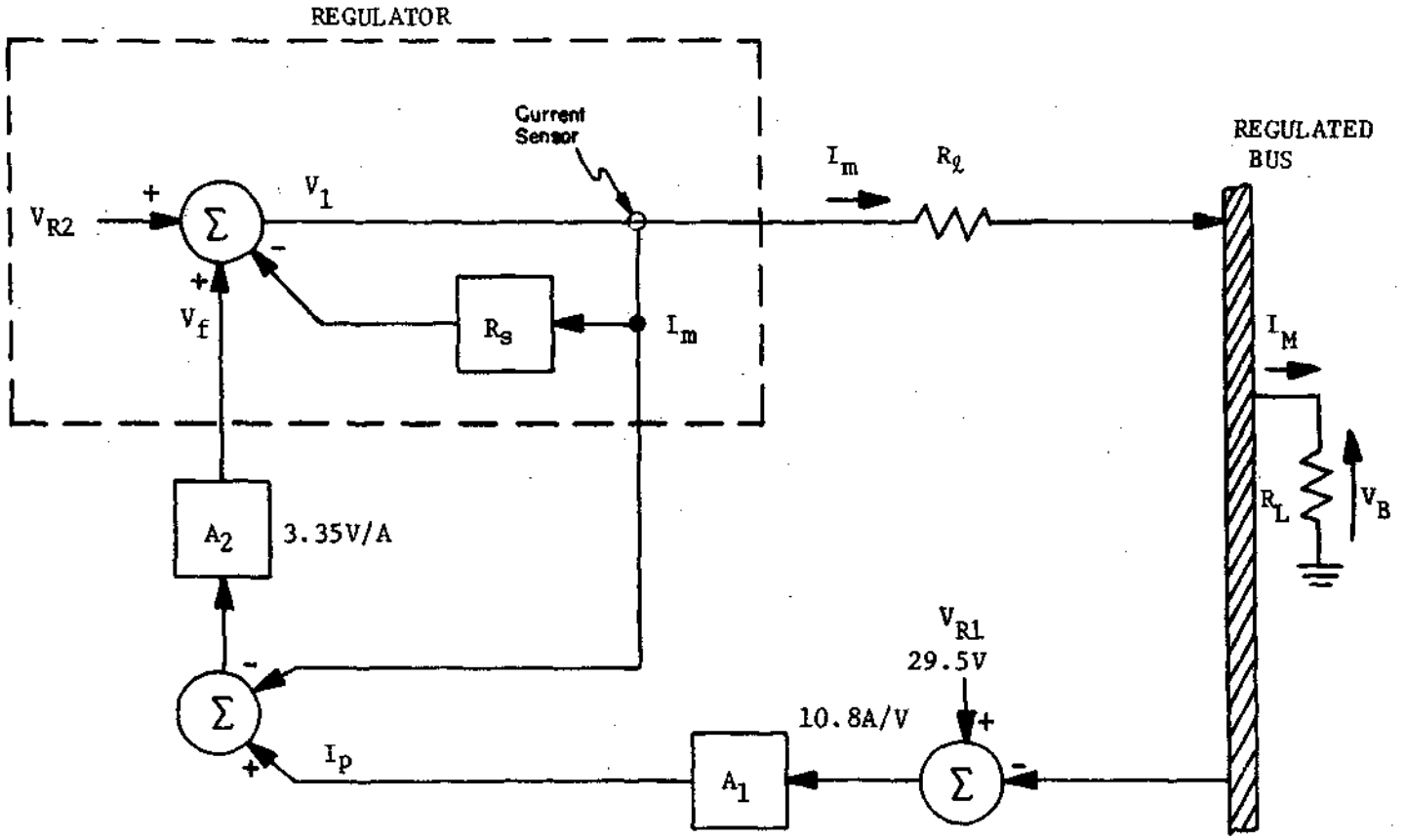

Figure 6-1. A feedback diagram of a regulator showing the power share scheme.

which has a value of 10.8 amperes per volt. The output of A_1 is regarded as a programmed current, I_p, and is used as a basis for comparison with the actual measured output current, I_m. The difference in I_p and I_m is amplified by A_2, whose value is 3.35 volts per ampere, and the resultant is V_f. Thus:

$$V_f = A_2[A_1(V_{R1} - V_B) - I_m] \quad . \tag{6-2}$$

The regulator output voltage then, with the feedback voltage, V_f, is

$$V_1 = V_{R2} - R_s I_m + V_f \quad . \tag{6-3}$$

The output bus voltage, V_B, will be equal to V_1 minus the voltage drop across R_ℓ, the distribution line resistance.

Any number of regulators can be paralleled as shown in Figure 6-2. Considering the i^{th} network, V_i is the output of the i^{th} regulator, $R_{\ell i}$ is the distribution line resistance of this i^{th} network, and I_{mi} is the current this network furnishes to the load. Each network has as amplifier with a gain of A_2 which will be considered the same for all regulators. To insure the same programmed current for all regulators, one reference voltage, V_{R1}, and one amplifier, A_1, are used. The sum of all the I_m currents equals I_M, the total current delivered to R_L, the load resistance. In the Skylab/ATM power system, there are eighteen regulators in parallel, but to conserve the generality of the following analysis, it will be assumed that n such regulators are in parallel.

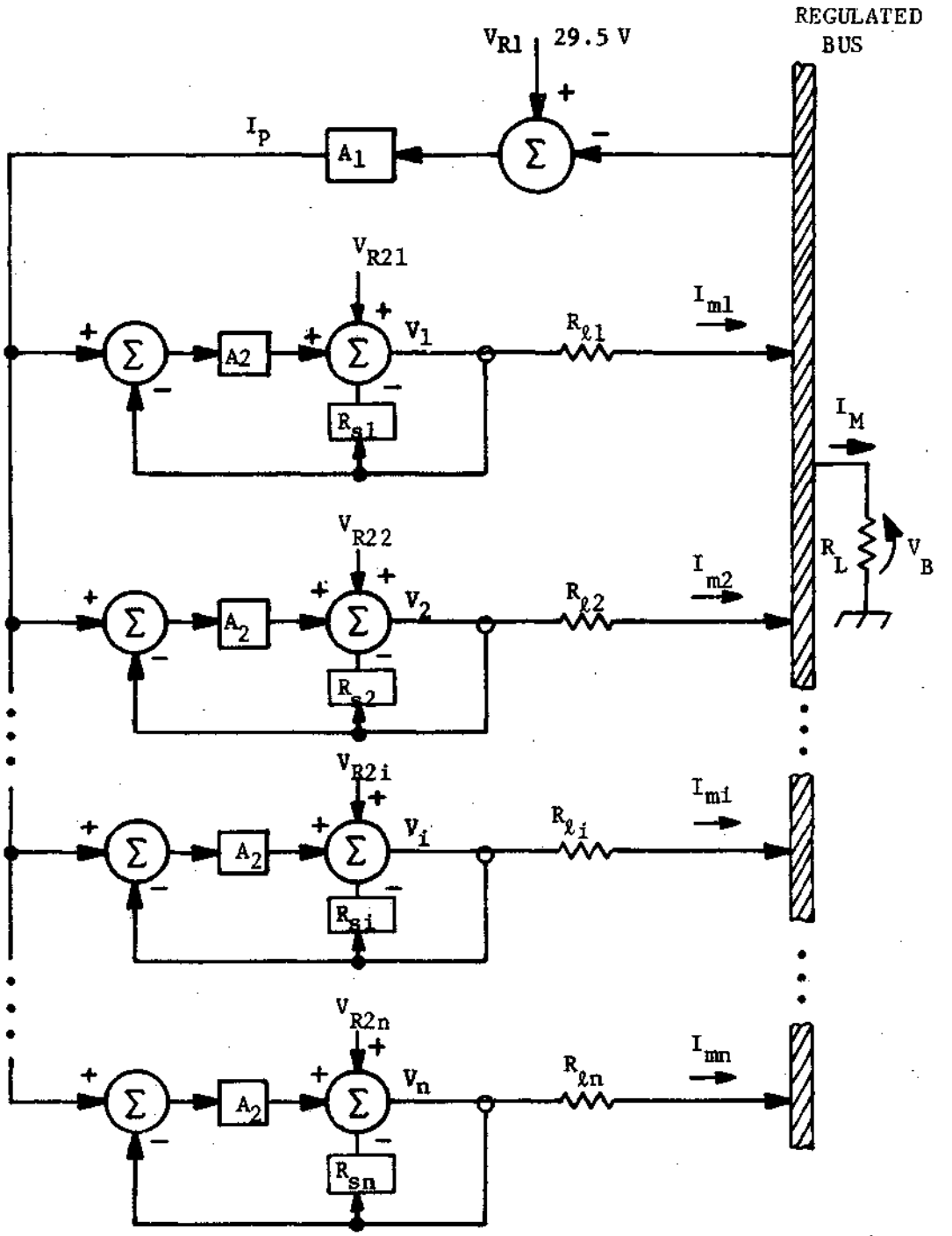

Figure 6-2. The arrangement for connecting n regulators in parallel.

A more useful feedback diagram will be constructed based on a relation for the bus voltage of n regulators in parallel, and the relationship obtained from this diagram will reveal the interaction among the regulators. The total output current, I_M, can be written as:

$$I_M = \frac{V_B}{R_L} = I_{m1} + I_{m2} + \ldots + I_{mi} + \ldots + I_{mn} \quad . \tag{6-4}$$

The individual currents, such as I_{mi}, can be replaced by an equivalent form.

$$I_{mi} = \frac{V_i - V_B}{R_{\ell i}} \tag{6-5}$$

Thus:

$$\frac{V_B}{R_L} = \frac{V_1 - V_B}{R_{\ell 1}} + \frac{V_2 - V_B}{R_{\ell 2}} + \ldots + \frac{V_i - V_B}{R_{\ell i}} + \ldots + \frac{V_n - V_B}{R_{\ell n}} \quad . \tag{6-6}$$

Solving for V_B yields:

$$V_B = \frac{R_L \sum_{i=1}^{n} V_i/R_{\ell i}}{1 + R_L \sum_{i=1}^{n} 1/R_{\ell i}} \quad . \tag{6-7}$$

Referring to Figure 6-2, it is seen that:

$$V_i = V_{R2i} + A_1A_2\ V_{R1} - A_1A_2\ V_B - (R_{si} + A_2)\ I_{mi} \quad . \tag{6-8}$$

Using Equation 6-5 and 6-8 in 6-7 yields:

$$V_B = \frac{R_L \sum_{i=1}^{n} \frac{V_{R2i} + A_1A_2\ V_{R1}}{R_{\ell i} + R_{si} + A_2}}{1 + R_L \sum_{i=1}^{n} \frac{1 + A_1A_2}{R_{\ell i} + R_{si} + A_2}} \quad . \tag{6-9}$$

By substituting Equation 6-8 into 6-5, an expression for the individual regulator output currents is obtained.

$$I_{mi} = \frac{V_{R2i} + A_1A_2\ V_{R1} - (1 + A_1A_2)\ V_B}{R_{\ell i} + R_{si} + A_2} \tag{6-10}$$

Using Equation 6-9, the final feedback diagram for n regulators in parallel is constructed and shown in Figure 6-3. The individual regulator output currents as well as the total output current are labeled.

To observe the relationship between bus voltage and output current, Equation 6-9 was used to calculate V_B for the possible range of load resistance. Identical regulators were assumed with line resistances of 50 milliohms. The results for different numbers of regulators in parallel are plotted in Figure 6-4. Noting the slope of the V_B/I_M

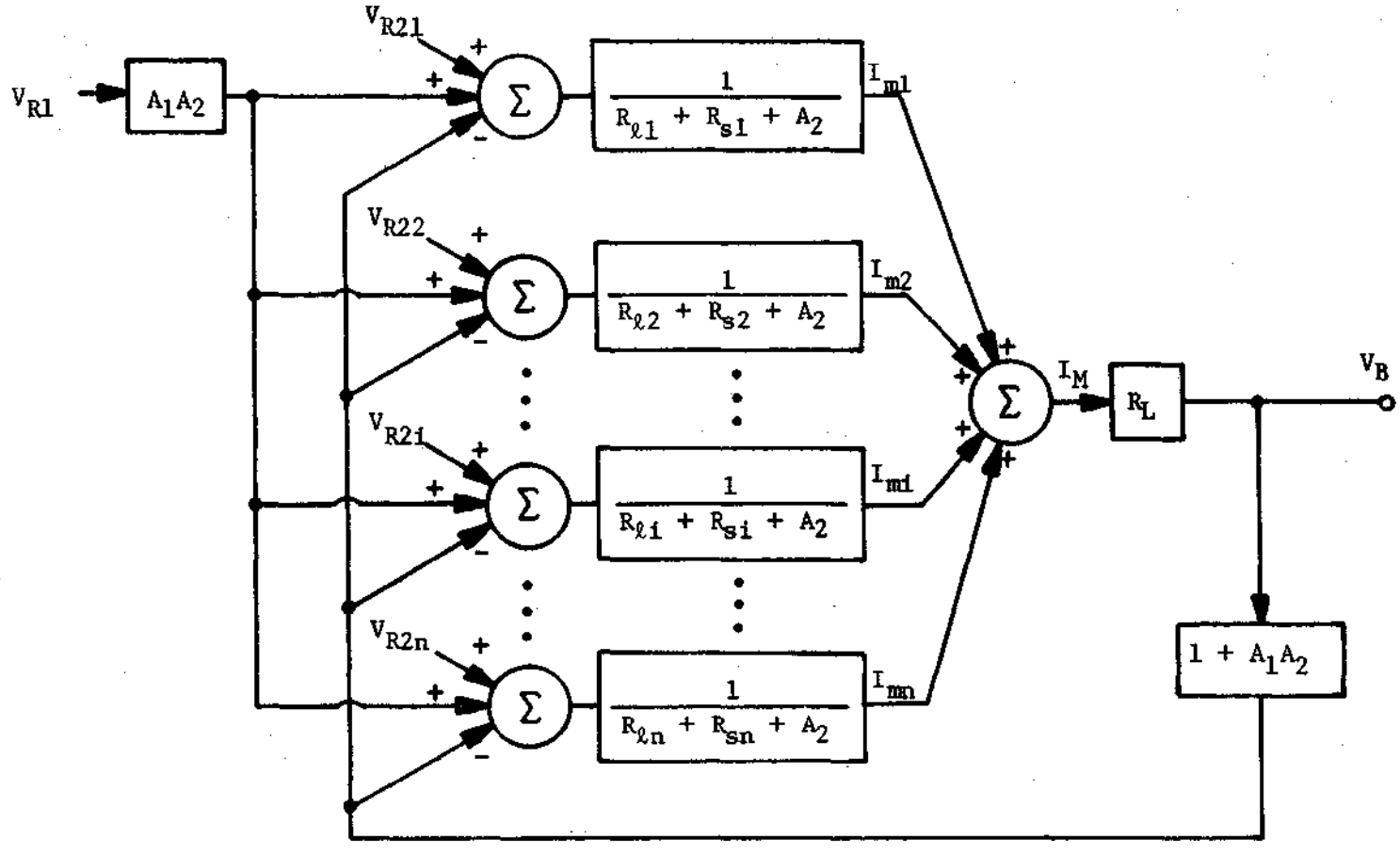

Figure 6-3. The final feedback diagram for n regulators in parallel.

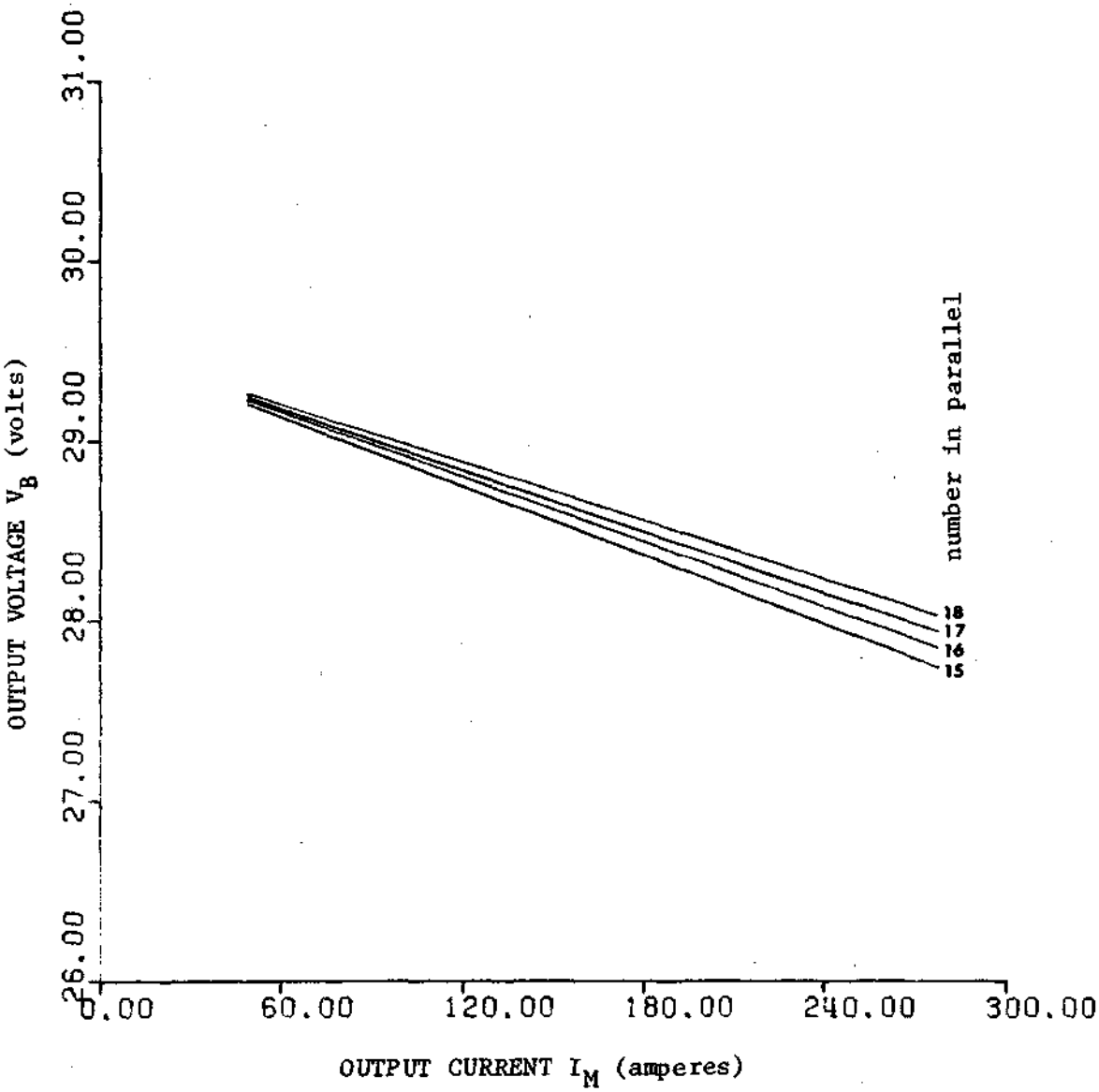

Figure 6-4. Regulation of paralleled regulators under power share control.

curve for eighteen in parallel, the system Thevenin resistance is approximately 5.6 milliohms. Thus, the new Thevenin resistance for each regulator, to be called R_s', is 18 times 5.6 milliohms or 100 milliohms. This can be shown mathematically by rewriting Equation 6-10 as:

$$V_B = \frac{1}{1 + A_1A_2} V_{R2i} + \frac{A_1A_2}{1 + A_1A_2} V_{R1} - \frac{R_{\ell i} + R_{si} + A_2}{1 + A_1A_2} I_{mi} \quad . \quad (6\text{-}11)$$

Now taking the derivative of V_B with respect to I_{mi} yields the new Thevenin resistance, R_{si}', of:

$$R_{si}' = \frac{R_{\ell i} + R_{si} + A_2}{1 + A_1A_2} \approx 97 \text{ milliohms.} \quad (6\text{-}12)$$

Figure 6-5 shows how the current in one regulator of 18 in parallel varies as a function of its line resistance. To create this figure, the line resistances of 17 of the regulators were set to 50 milliohms and the resistance of the eighteenth was varied from 10 milliohms to 110 milliohms.

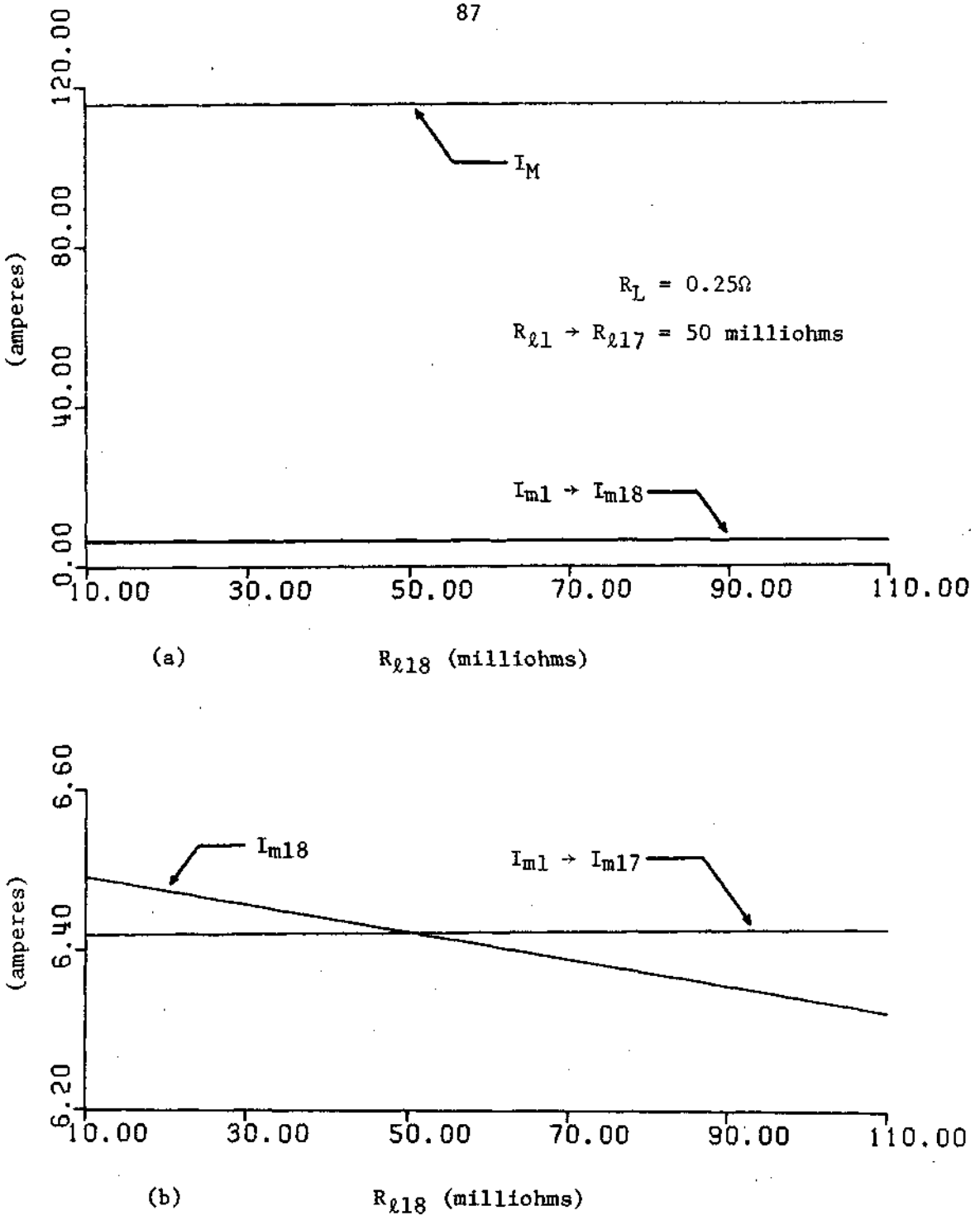

Figure 6-5. (a) The output current of each regulator and the total output current, I_M. (b) An expanded view of the individual regulator currents.

VII. RESULTS AND CONCLUSIONS

This chapter presents some of the results that were obtaimed through the computer program model of the regulator. The results are in the form of graphs created from data generated by the program and are an indication of the type of information that can be obtained.

First, for a variety of load resistances, the different switching times are plotted as a function of input voltage. Figure 7-1 shows the characteristic of TCHARG, the on time of the switching transistors, and Figure 7-2 shows the characteristic of TDUMP, the dump time for the charging inductors. The off time, TDWELL, is shown in Figure 7-3. The displacement of the 2 and 4 ohm load curves is due to the large currents flowing through the charging inductors during TCHARG. The large values of current causes the inductance value to decrease (approach saturation) resulting in a further increase in current. The outcome is current values which are larger than would be if the inductor did not approach saturation, and this in turn produces sufficient output voltage to require the regulator to remain in the off state longer.

Figure 7-4 shows how the duty cycle, D, of the switching transistors is a function of the input voltage and the load resistance. Closely related to this is the information in Figure 7-5. This is the switching repetition rate of the regulator as a function of load resistance for two different input voltages. The shape of the curves is due

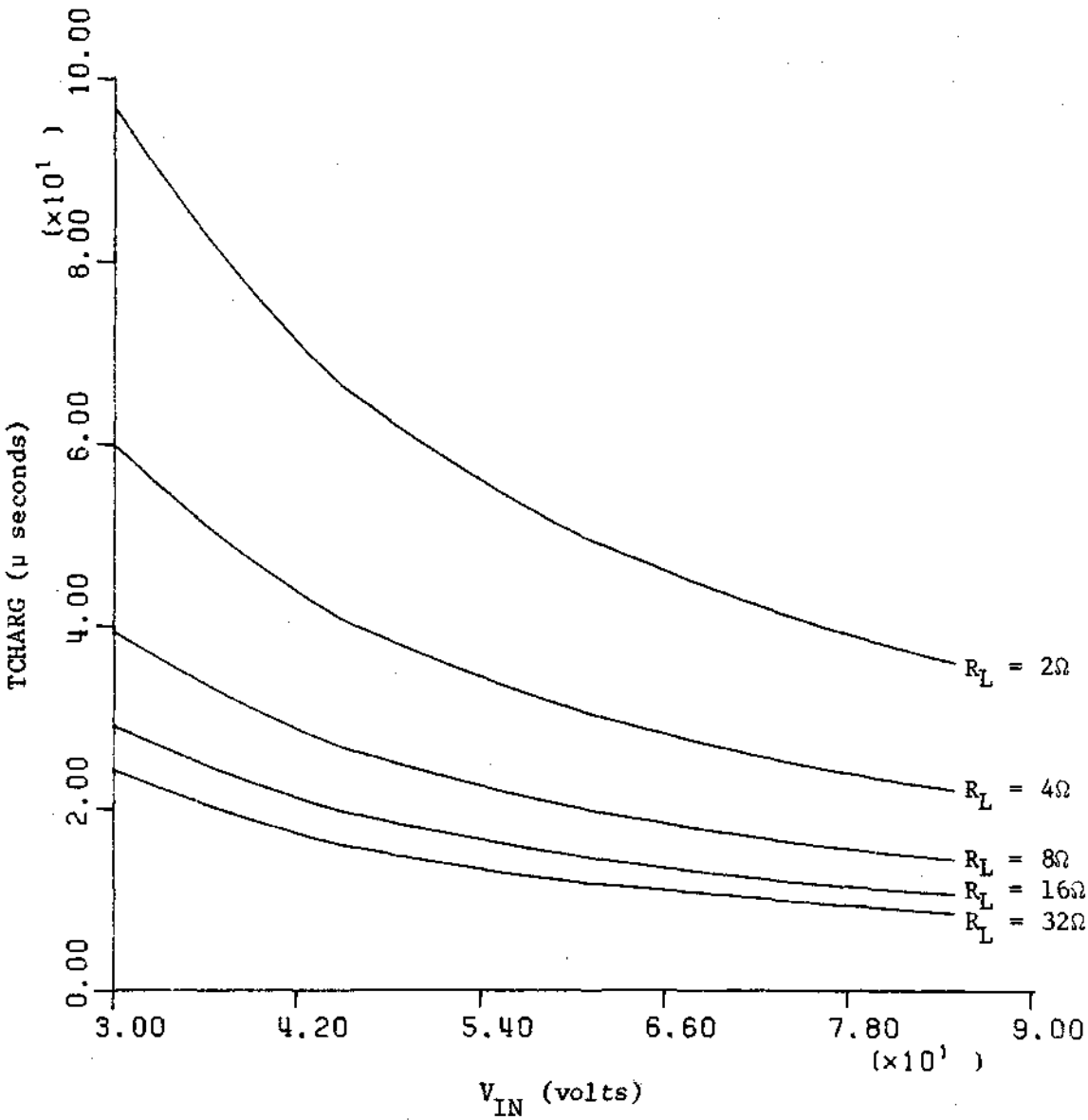

Figure 7-1. On time, TCHARG, as a function of input voltage and load resistance.

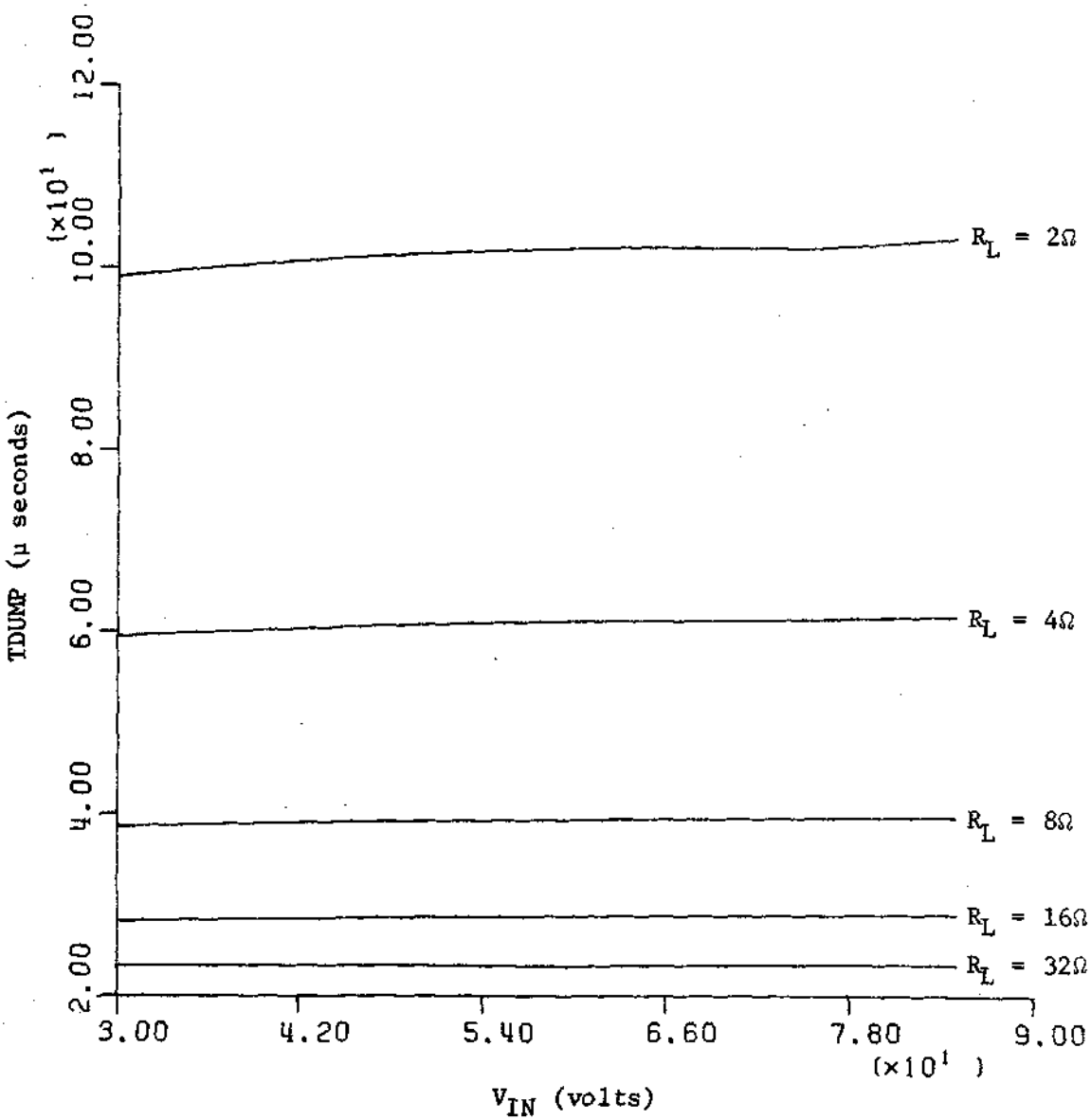

Figure 7-2. Dump time, TDUMP, as a function of input voltage and load resistance.

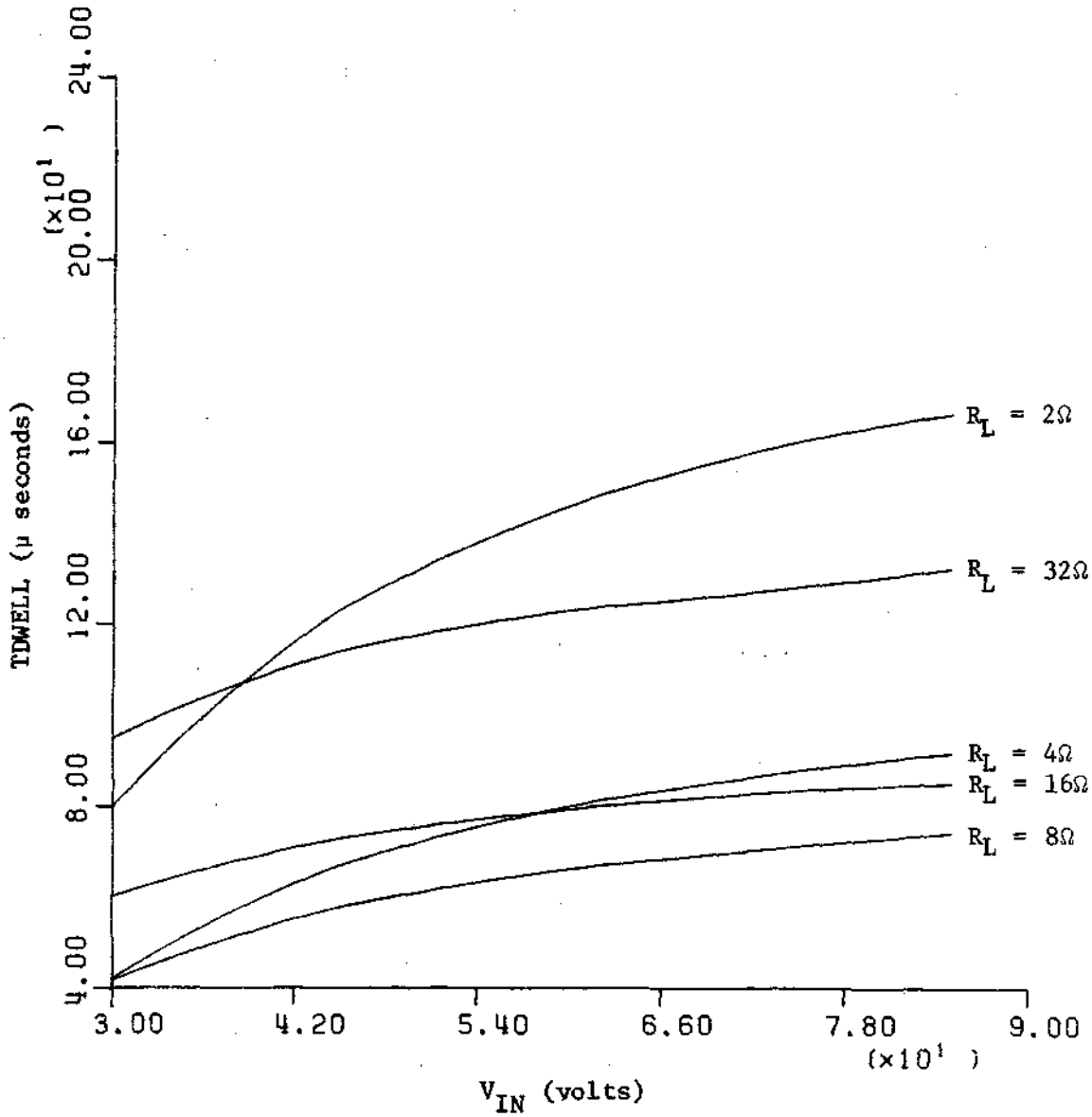

Figure 7-3. Dwell time, TDWELL, as a function of input voltage and load resistance.

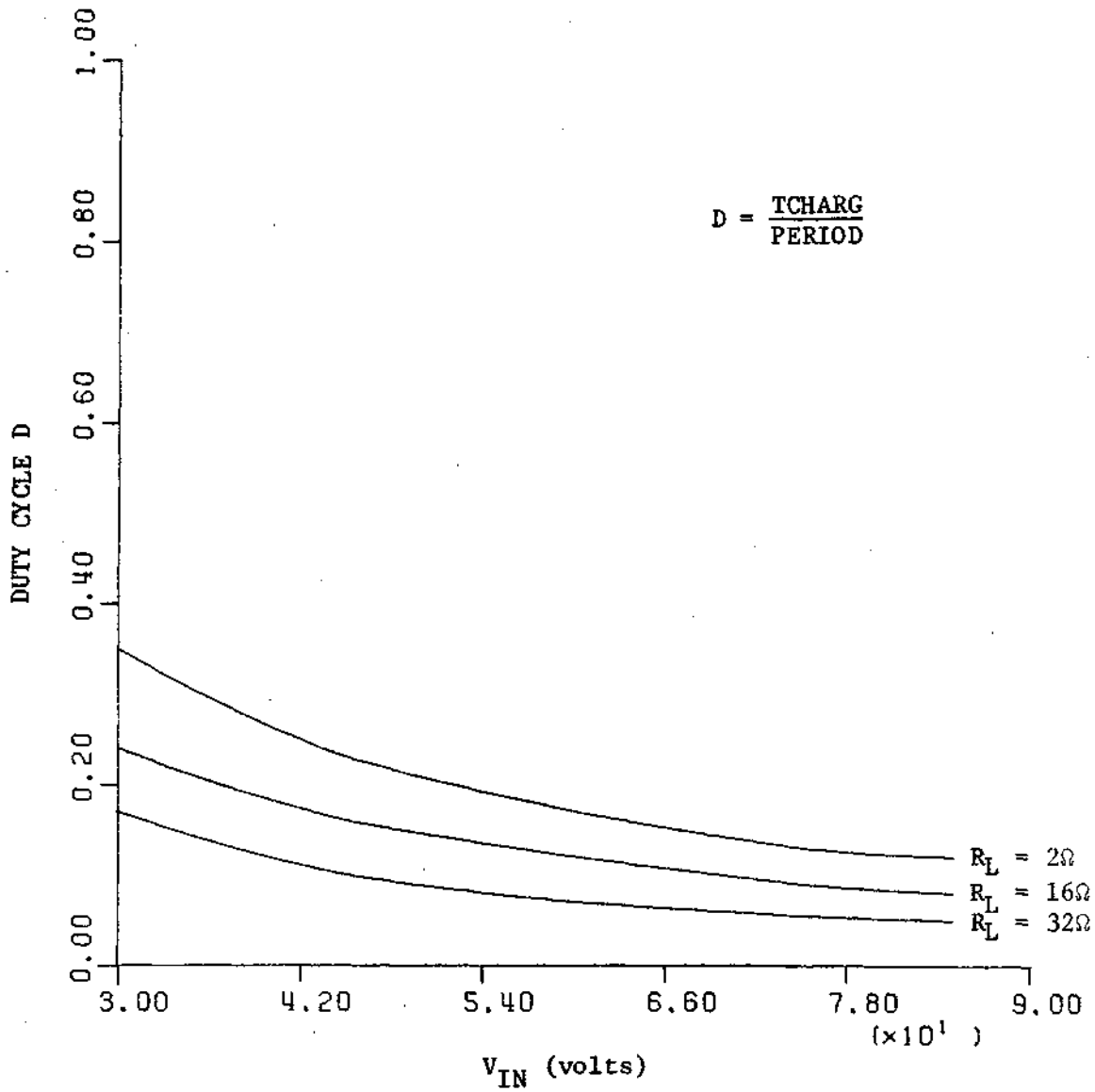

Figure 7-4. Duty cycle of switching transistors as a function of input voltage and load resistance.

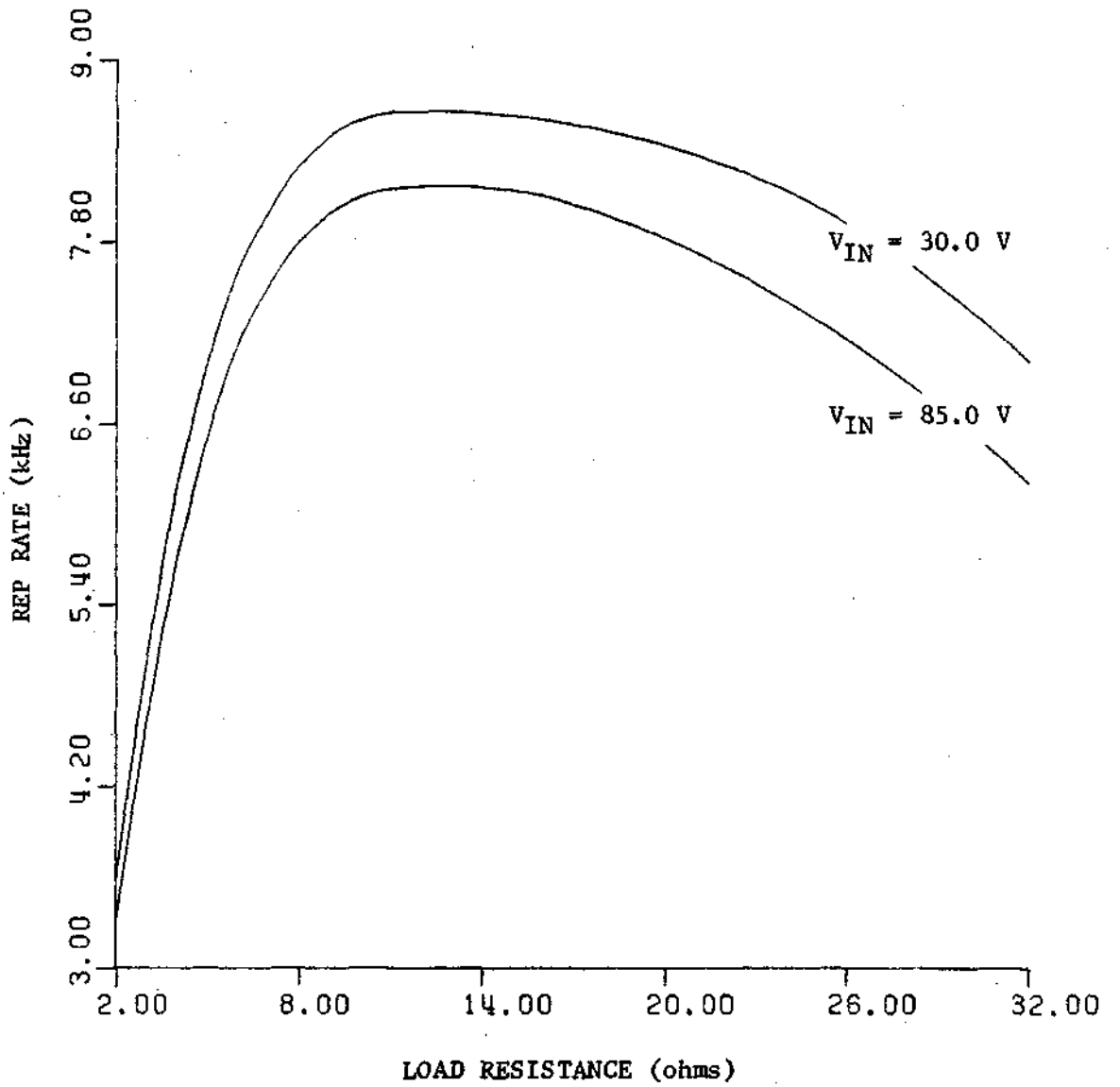

Figure 7-5. Repetition rate of switching transistors as a function of load resistance and input voltage.

to the nonlinear decrease in TCHARG, TDUMP and TDWELL as the load resistance increases. For values of R_L above 8 or 10 ohms, the decrease becomes small for TCHARG and TDUMP while TDWELL begins to increase.

The transient response of the regulator, with zero initial conditions, is exhibited in Figures 7-6 and 7-7. In Figure 7-6, each pulse of current shown is due to the charging inductors dumping their energy into the output filter. It is recalled that each regulator has four such inductors in parallel and the dump current, I_{DUMP}, will be the sum of their currents. The damped oscillation in I_2, the current in the middle loop of the filter, is due to the natural response of the filter and has a frequency of approximately 250 Hz. Since the magnitude of this current is used to determine TCHARG, the oscillation is passed to I_{DUMP} after a small time delay. Initially, the output voltage is low enough to require the transistor switches to turn on immediately after the charging inductors have dumped. Thus the dwell time, TDWELL, is zero. The change in disposition of the current pulses near 10 milliseconds is due to the voltages of the filter becoming large enough to allow the regulator to dwell before requiring the switches to turn on.

Figures 7-8 and 7-9 contain the steady-state response of the regulator to a 4Ω load and a 60 volts input. The scales of the plots have been expanded beyond those of the transient response to disclose more detail. The small change in rate of decrease of the dump current, I_{DUMP}, (see last current pulse) is due to the change in inductance of the charging inductor. Later, another figure will examine the effect of this inductor on current and time values more closely. The ripple voltage at the input of the output filter is seen in Figure 7-9. The near

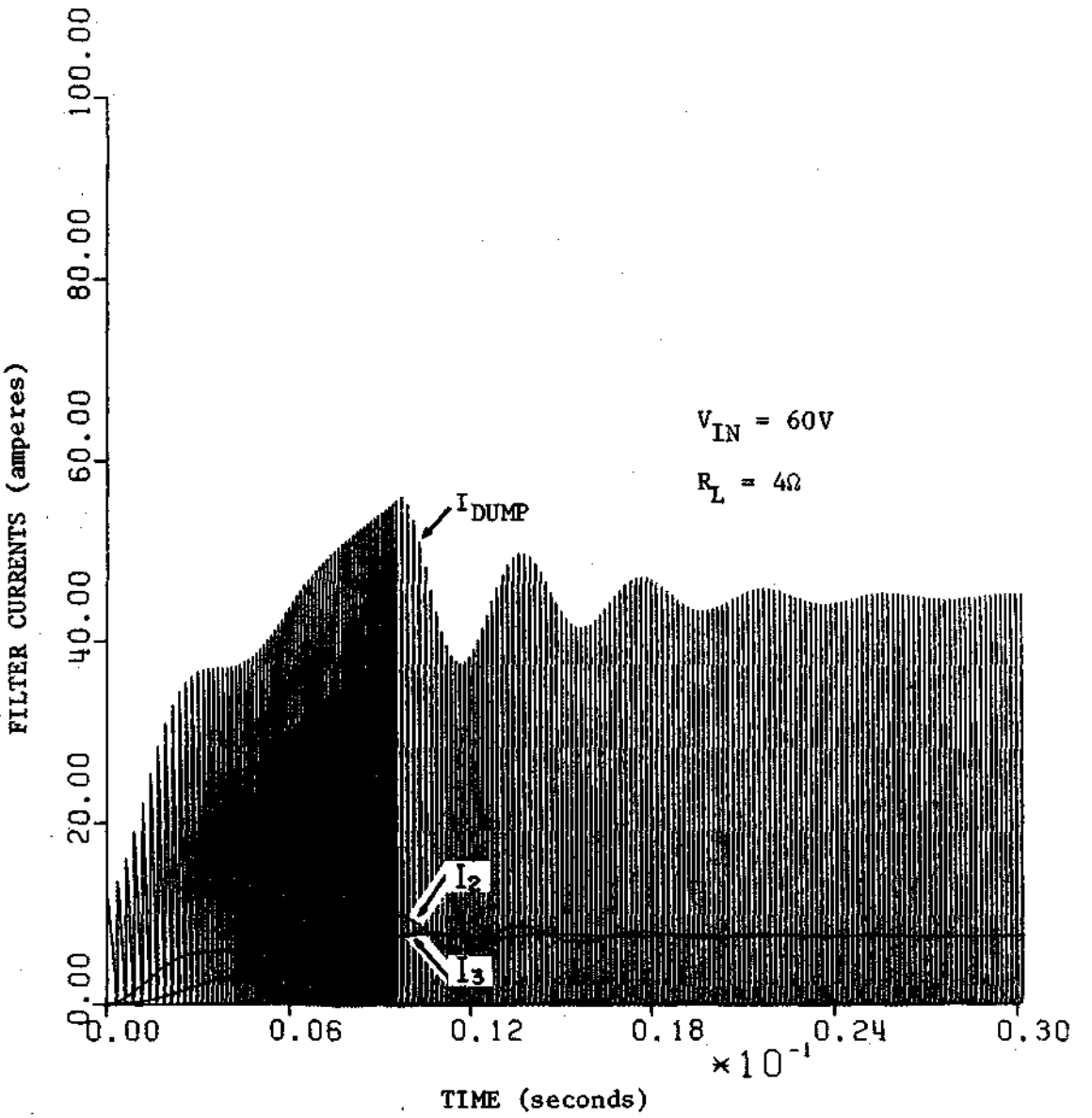

Figure 7-6. Transient response of filter currents.

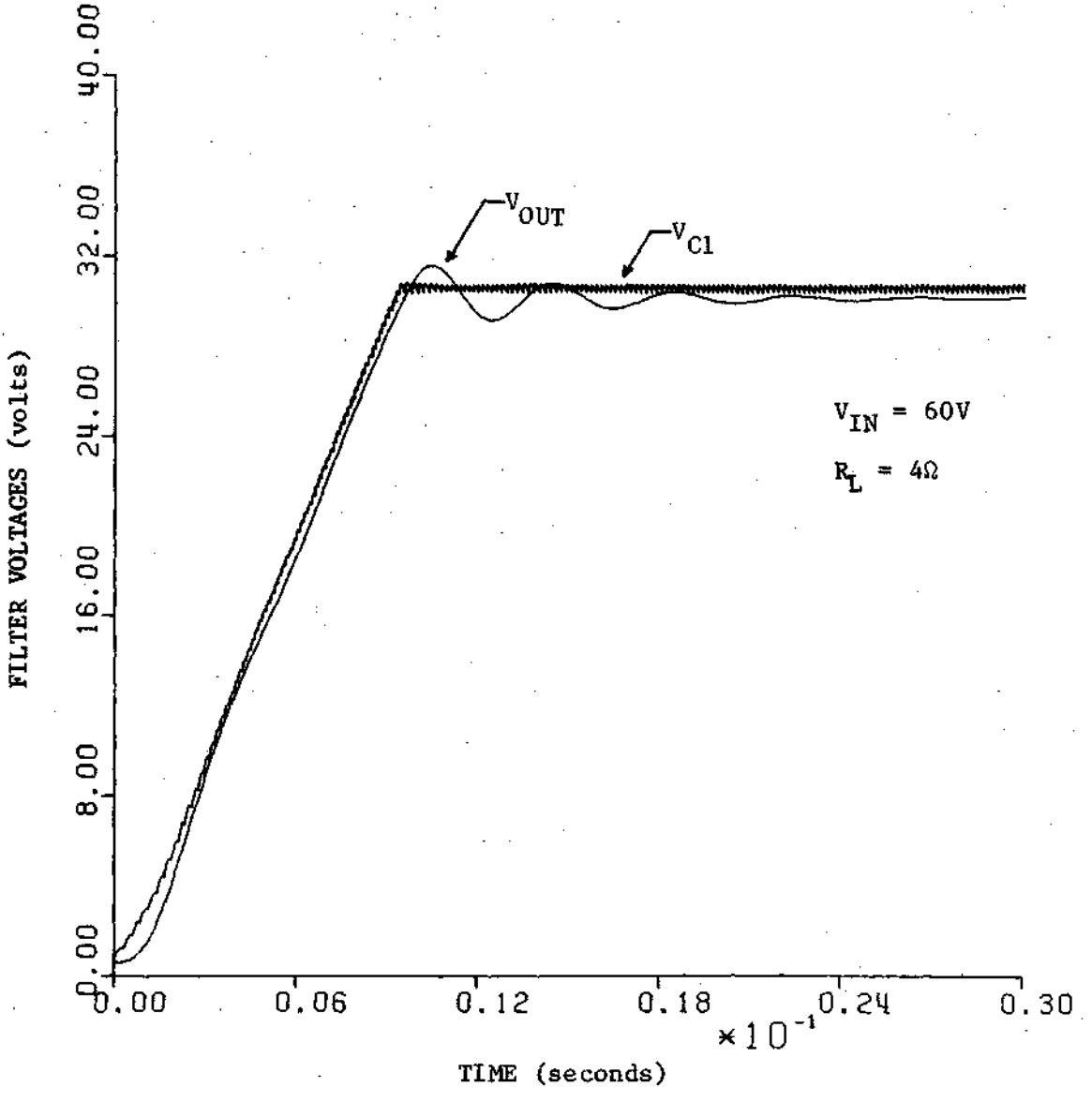

Figure 7-7. Transient response of filter voltages.

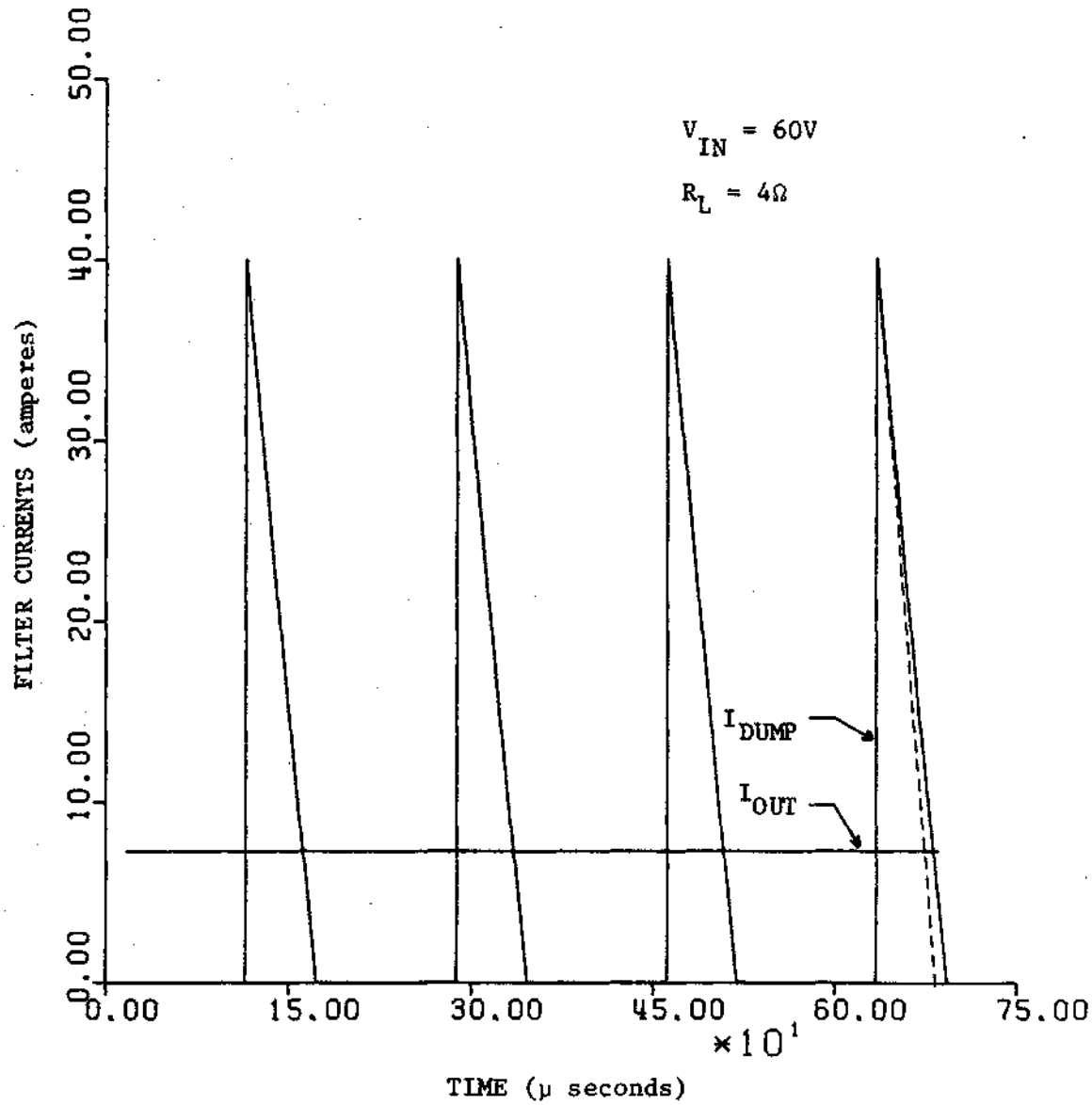

Figure 7-8. Steady-state response of filter currents.

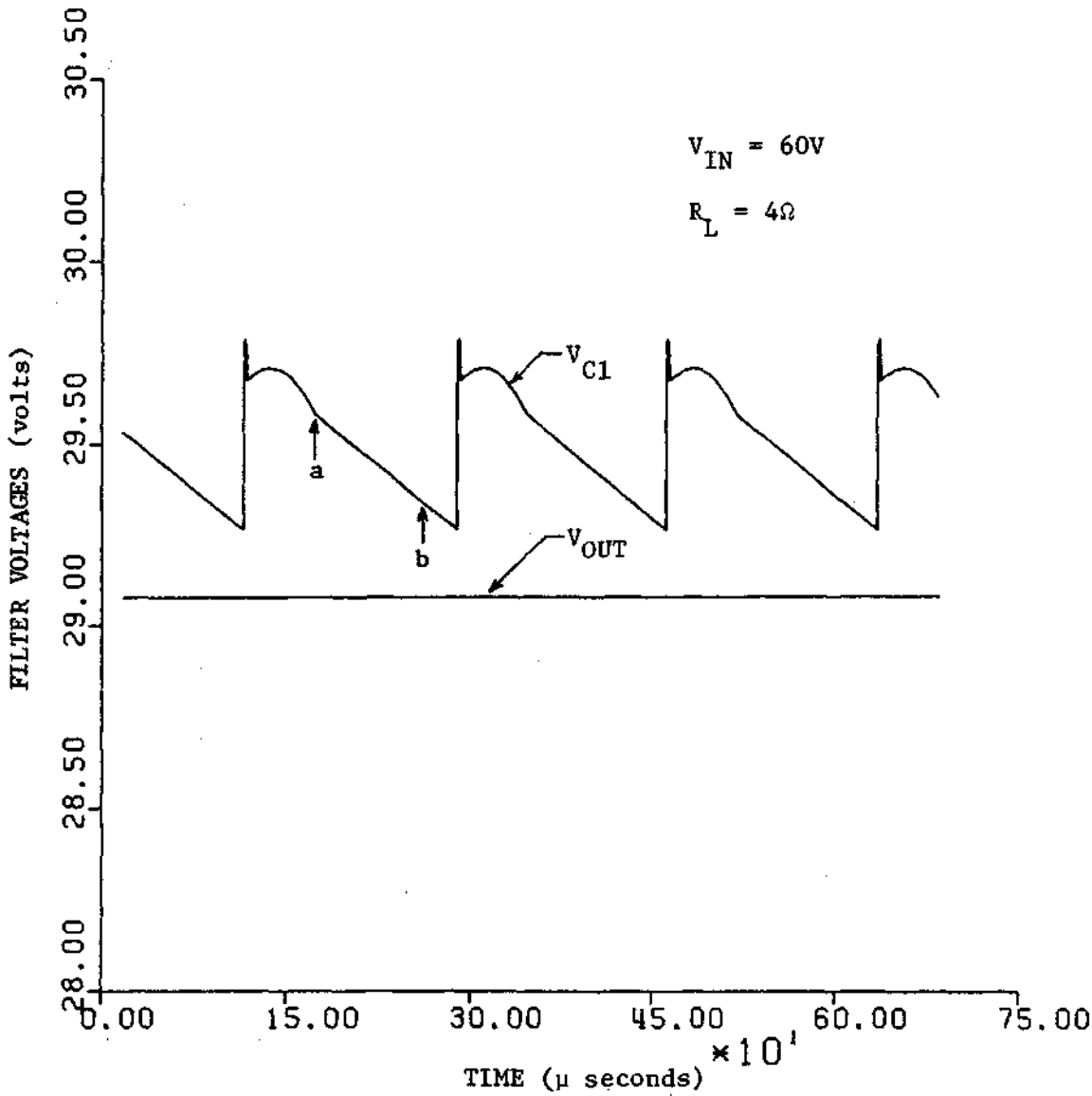

Figure 7-9. Steady-state response of filter voltages.

instantaneous jump in V_{C1} takes place just as the transistor switches begin to turn off and the charging inductors begin to dump. Its magnitude is composed of two voltage terms. First, the voltage across R_{C1}, the effective resistance of the branch containing C1, and, second, the voltage across L_{C1}, the effective inductance of the same branch. The spike component at the jump is the voltage across L_{C1} and the rest of the jump is due to the voltage across R_{C1}. As explained in Chapter III, the duration of the spike is equal to the turn-off time of the switching transistors, which is less than one microsecond.

The end of TDUMP and beginning of TDWELL is indicated by point "a" on the plot, and the end of TDWELL and beginning of TCHARG is indicated by point "b". The fact that the voltage across C1 doesn't appear exponential during the discharge time, TDWELL plus TCHARG, is due to the large time constant present.

A plot of output voltage versus output current is given in Figure 7-10. The slope is due to the effective internal dc resistance of 213 milliohms programmed into the regulator by the use of current feedback.

To show the nonlinear charging and discharging currents, Figure 7-11 is now presented. This represents the worse case in that the regulator is working under the maximum current demand allowed, 15.5 amperes. The value of I_{DUMP} is the sum of the four currents coming from the four charging inductors. The dashed line indicates the charging current possible during TCHARG for the ideal case in which the inductor's value does not decrease.

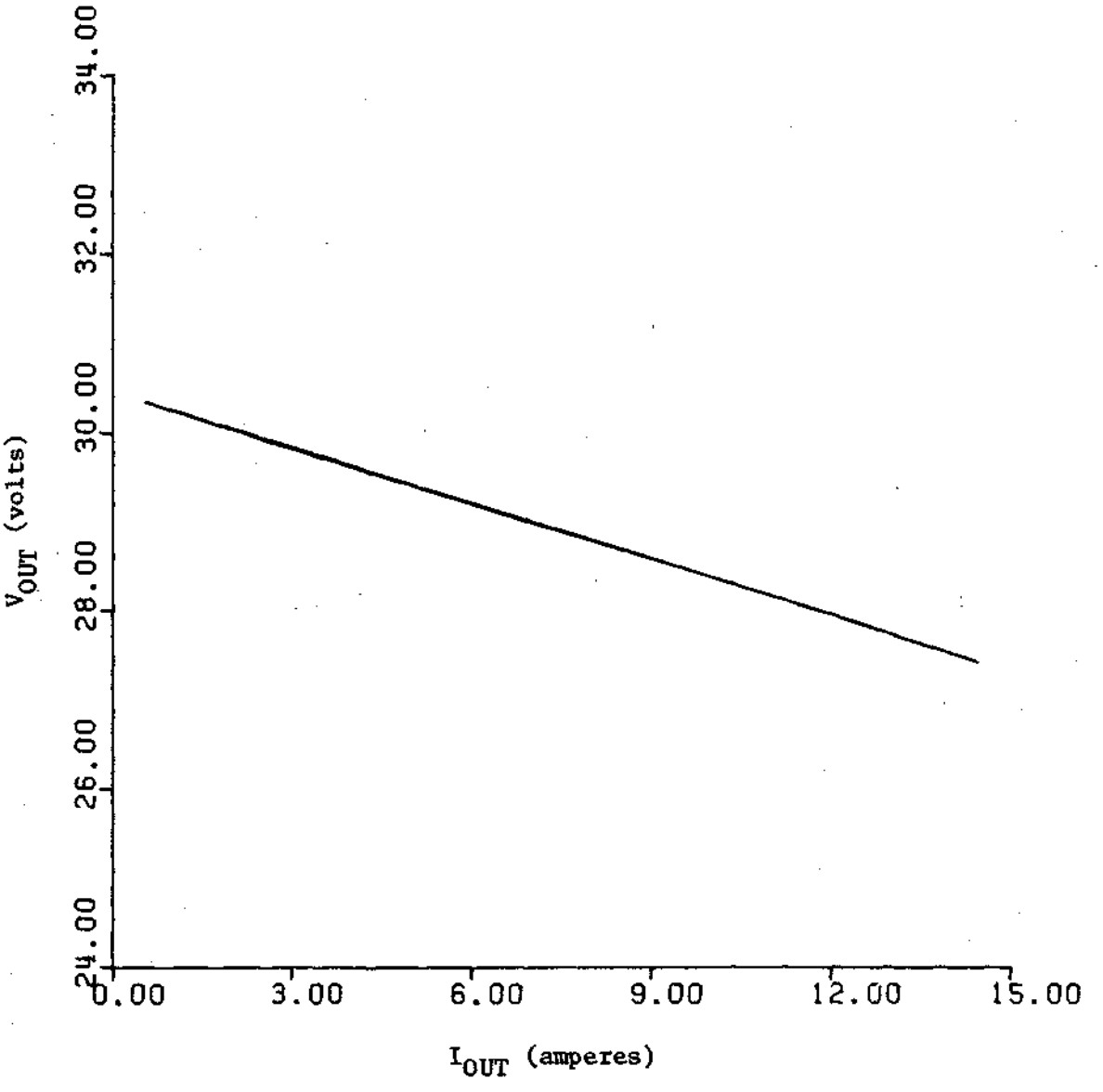

Figure 7-10. Output voltage/output current characteristic of regulator model.

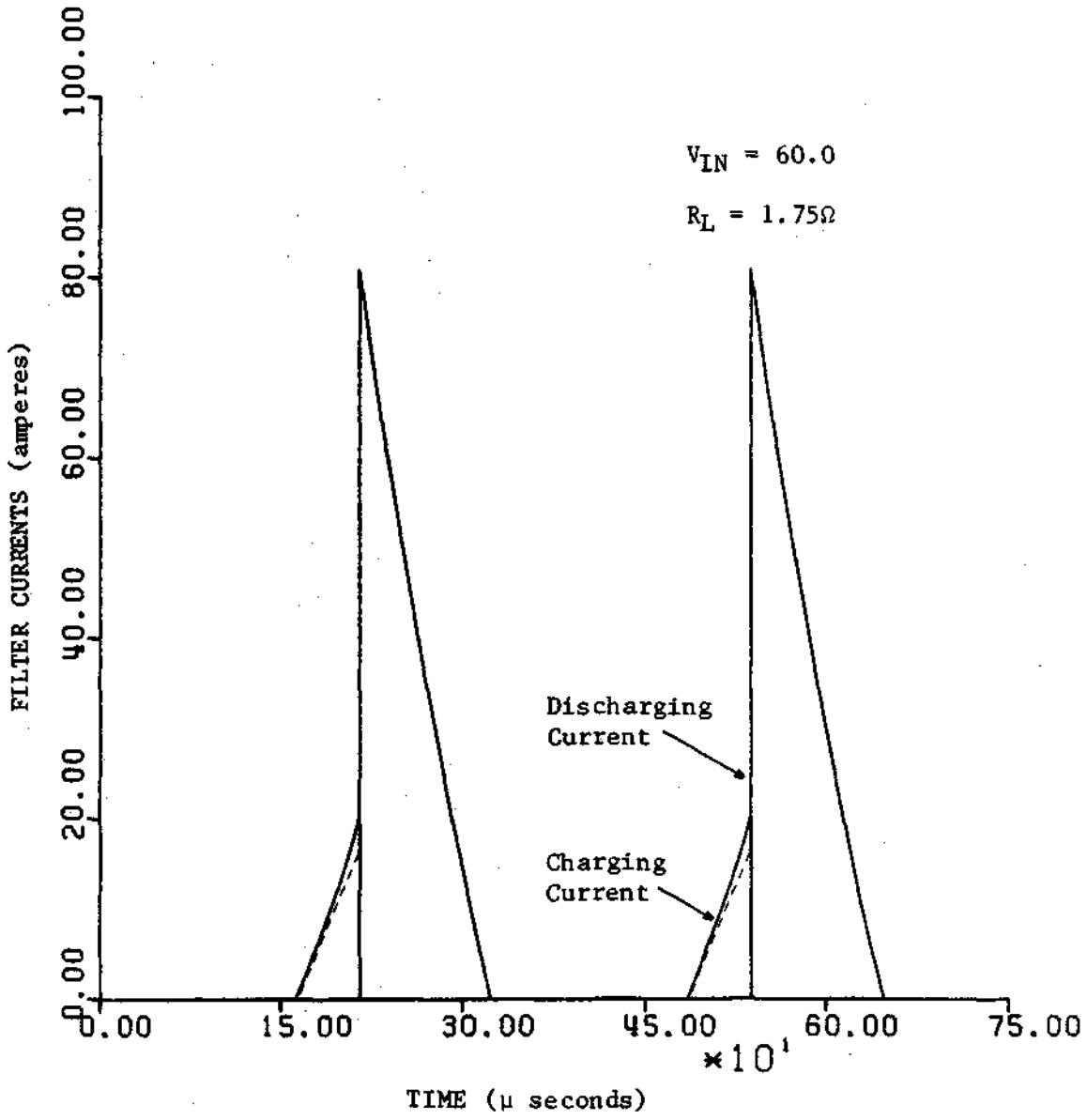

Figure 7-11. Current input to the charging inductors and, I_{DUMP}, total current dumped into output filter.

The last four figures contain the response of the regulator to a sudden change in load resistance. Figures 7-12 and 7-13 show the results of the regulator, under steady-state conditions, having the load resistance switched from 4 ohms to 2 ohms. Figures 7-14 and 7-15 are for the load being switched from 4 ohms to 8 ohms.

The intent of the preceding fifteen figures was to display a sample of what can be accomplished with the computer program and at the same time familiarize the reader with some of the CBRM's characteristics.

This report is concluded by summarizing what has been accomplished. The necessary mathematical expressions were developed in Chapter III to represent the three switching times: TCHARGE, TDUMP, and TDWELL. Using the results of Chapter III, a computer program model was developed and presented in Chapter IV. The guidelines stated in the Introduction were followed closely and the result was a very versatile program that can easily be modified to examine any particular area of interest. For example, in addition to what was done at the beginning of this chapter, it is possible to investigate the effect of varying a component value over a large range.

There are at least two areas that could be investigated further. First, in modeling the spike present in V_{C1} several simplifying assumptions were made. To be more exact, information is needed on the effective inductance at the input of the output filter and a good equivalent model of the switching transistor is necessary. A second area is the calculation of the ac output impedance for very low frequencies. Due to the presence of nonlinearities, linear or piecewise-linear methods

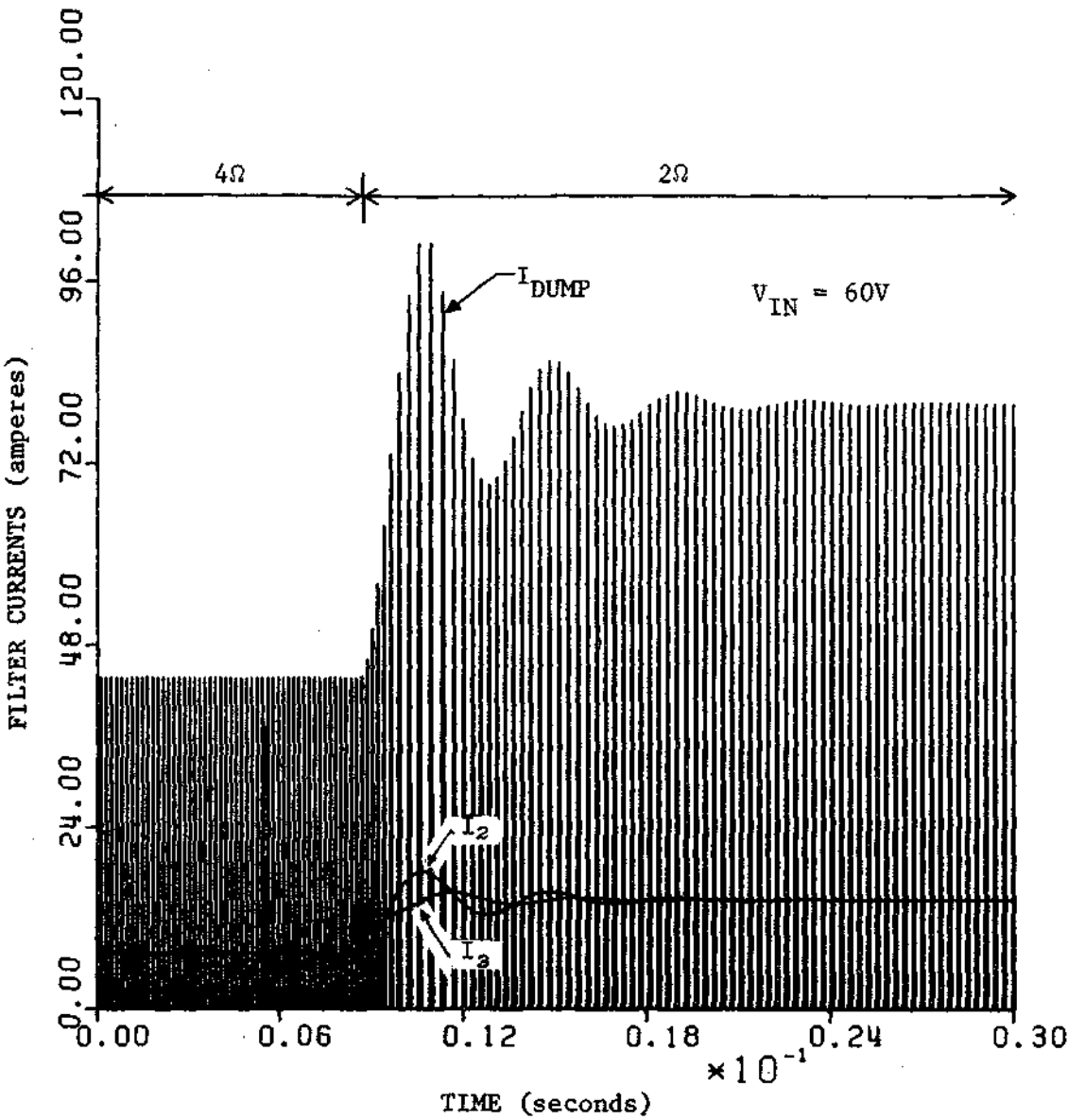

Figure 7-12. Transient response of filter currents to a 4 ohms-to-2 ohms load change.

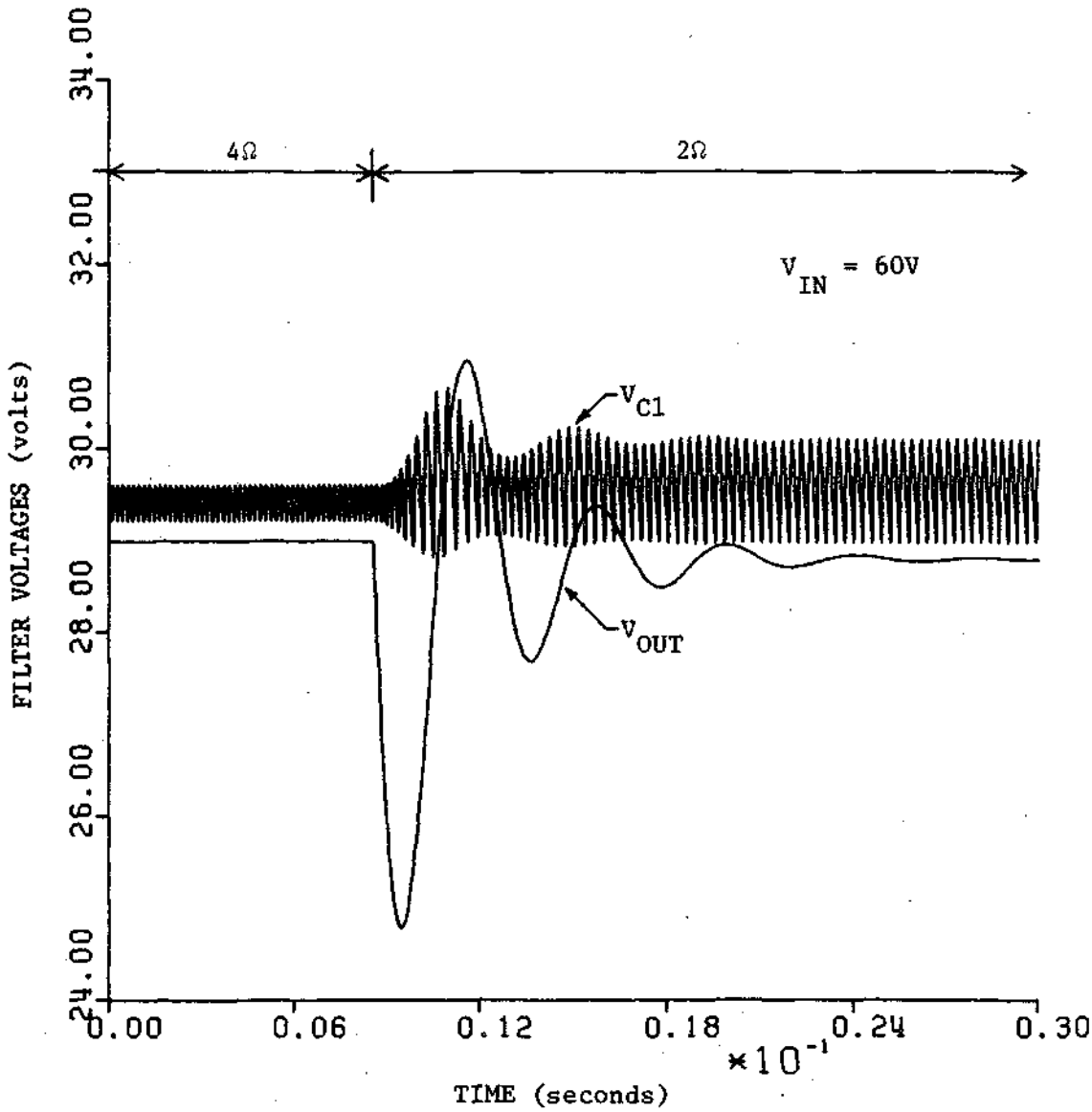

Figure 7-13. Transient response of filter voltages to a 4 ohms-to-2 ohms load change.

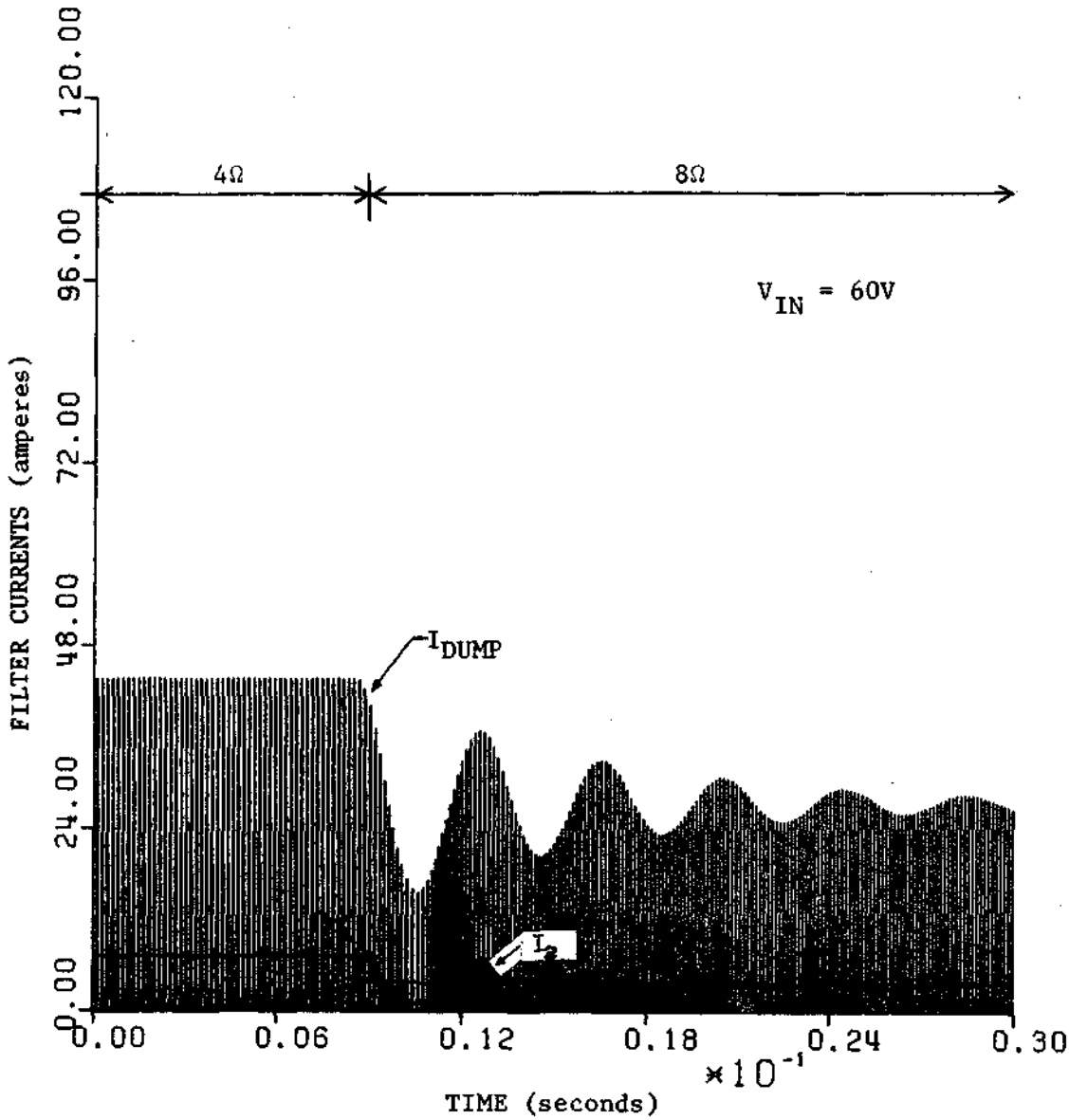

Figure 7-14. Transient response of filter currents to a 4 ohms-to-8 ohms load change.

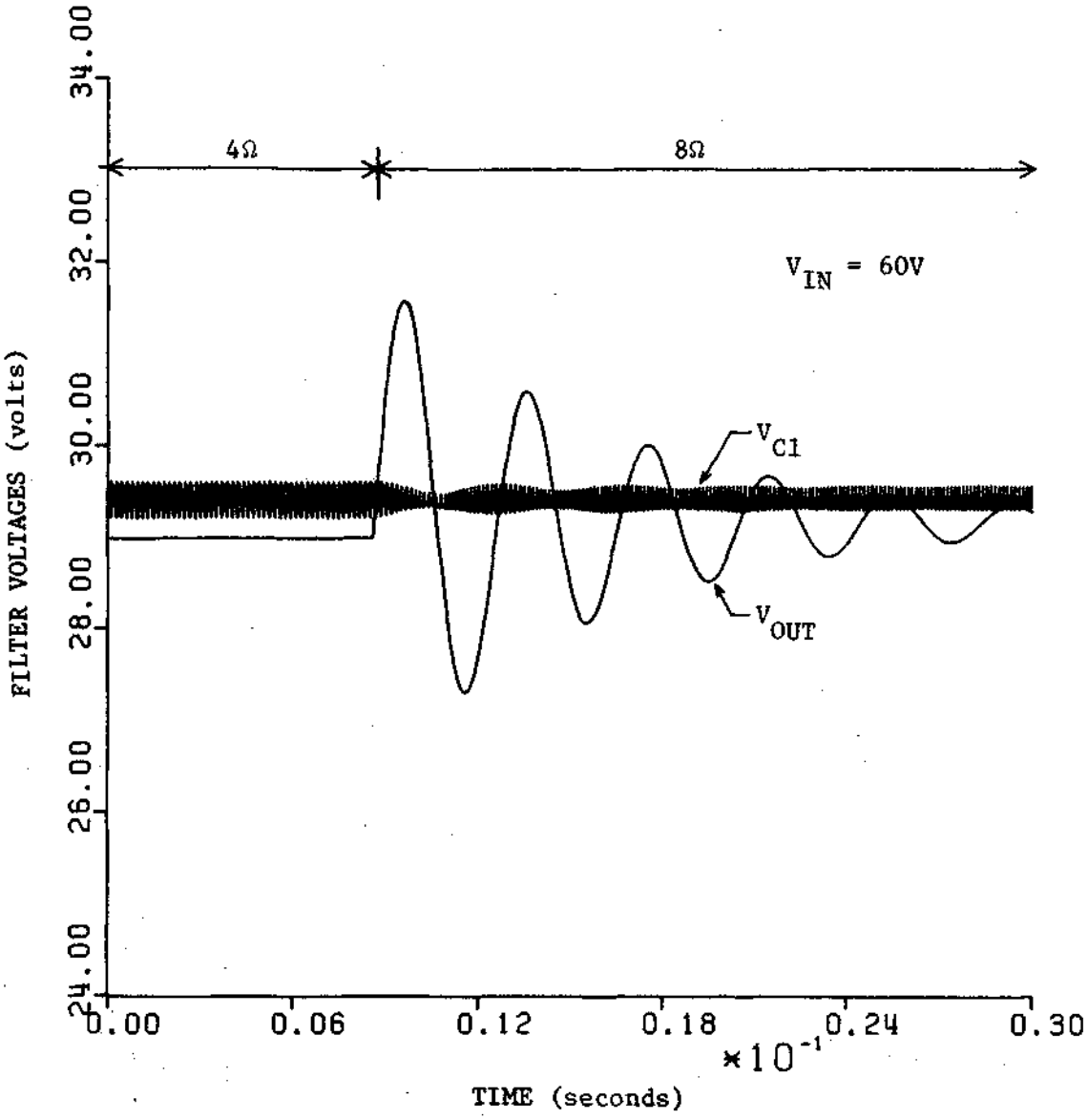

Figure 7-15. Transient response of filter voltages to a 4 ohms-to-8 ohms load change.

could not be used.

Two areas that were not covered in this report are, 1) calculations of efficiency of power transfer, and 2) an investigation of a damped high frequency oscillation that last for a short duration when the charging inductors dump. To calculate efficiency, the power loss in the switching transistors must be calculated and given sufficient information, this can be done. To analyze the oscillation, the stray capacitance and inductance must be known.

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APPENDIX A

The development of Equation 3-2 of Section A, Chapter III, repeated below as Equation A-1, will be done by solving for I_{A1}.

$$I_A(S) = \frac{-V_D}{R_D + R_{L1} + R_{L2} + R_L} \frac{1}{S} + \frac{a_3S^3 + a_2S^2 + a_1S^1 + a_0}{b_4S^4 + b_3S^3 + b_2S^2 + b_1S^1 + b_0} \quad \text{(A-1)}$$

The form of I_{A2} and I_{A3} will be as that of I_{A1}. The matrix expression for the filter currents was given in Equation 3-1 and using Cramer's rule for the solution of equations will yield:

$$I_{A1}(S) = \frac{D_1}{D} = \frac{A_4S^4 + \cdots + A_1S - V_D}{S(b_4S^4 + \cdots + b_1S + b_0)} \quad \text{(A-2)}$$

The above equation can be expanded into two terms.

$$I_{A1}(S) = \frac{K_1}{S} + \frac{K_2}{b_4S^4 + \cdots + b_1S + b_0} \quad \text{(A-3)}$$

Solving for K_1 and K_2 yields:

$$K_1 = -\frac{V_D}{b_0} \tag{A-4}$$

and

$$K_2 = (A_4S^3 + \cdots + A_1) + \frac{V_D}{b_0}(b_4S^3 + \cdots + b_1) \tag{A-5}$$

It is noticed that the first term of K_2 is the numerator of D_1/D with the last term deleted and the powers of S decreased by one. In addition, the second term of K_2 is V_D/b_0 times the denominator of D_1/D with the last term deleted and the powers of S decreased by two. Using this approach, the K_2's are calculated and called CNUMA in the computer program.

APPENDIX B

In this section, the parameters of Equation 3-4, repeated below, are discussed.

$$i_A(t) = 2R_{A1} \exp[-\alpha_{A1}t] \cos(\omega_{A1}t + \theta_{A1}) + 2R_{A2} \exp[-\alpha_{A2}t] \cos(\omega_{A2}t + \theta_{A2}) - V_D/(R_D + R_{L1} + R_{L2} + R_L) \quad \text{(B-1)}$$

This equation represents the form of the three loop currents of the output filter while it is in mode A. The notation used below is the same as that used in the computer program.

The three currents are called CURNT(1), CURNT(2), and CURNT(3) in the computer program and each subscript, (1), (2), and (3) refers to a particular loop in the filter. The method of the Heaviside partial fraction expansion can be programmed to determine the parameters of these three currents. First, there are six RA's to be found which are the magnitudes of the coefficients of the partial fraction expansion. They will be double subscripted showing first the current to which they belong and second showing position within that current equation. Thus the six RA's are:

RA(1,1) , RA(1,2)

RA(2,1) , RA(2,2)

RA(3,1) , RA(3,2)

In general, the magnitude RA_i for a complex root can be found from:

$$CKA_i = RA_i \angle \theta A_i = \left[(S + \alpha A_i - j\omega A_i) \frac{P(S)}{Q(S)}\right]_{S = -\alpha A_i + j\omega A_i} \quad \text{(B-2)}$$

Using this approach for example, R(1,1) will be:

$$\left|CKA(1,1)\right| = RA(1,1) = \left|\frac{CNUMA(1,k)}{DNOMA(k)}\right| \quad \text{(B-3)}$$

where CNUMA(1,k) is the numerator of the polynomial fraction in $I_{A1}(S)$ evaluated at S equal to $-\alpha A1 + j\omega A1$. DNOMA(k) is the denominator of the polynomial fraction in $I_{A1}(S)$ less the $S + \alpha A1 - j\omega A1$ factor, evaluated at S equal to $-\alpha A1 + j\omega A1$.

The αA's, called ALPHAA(1) and ALPHAA(2) in the program, are equal to minus the real parts of the complex roots used to determine the RA's. The ωA's, called OMEGAA(1) and OMEGAA(2) in the program, are the positive imaginary parts of the complex roots used to determine the RA's. Note that each current equation will contain the two αA's and ωA's.

The θA's are the phase angles associated with the coefficients of the partial fraction expansion that were used in determining the RA's. They will be double subscripted showing first the current to which they belong and second showing position within that current equation.

The six θA's are

THETAA(1,1) , THETAA(1,2)

THETAA(2,1) , THETAA(2,2)

THETAA(3,1) , THETAA(3,2)

They can be found by taking the arctangent of the imaginary part of the coefficients used in determining the RA's divided by its real part. For example:

$$\text{THETAA(1,1)} = \text{Arctan}\left[\frac{Imag(\text{CKA(1,1)})}{Re(\text{CKA(1,1)})}\right] \qquad \text{(B-4)}$$

The procedure used in finding the parameters for the mode A current equations is used to find those belonging to the equations for mode B.